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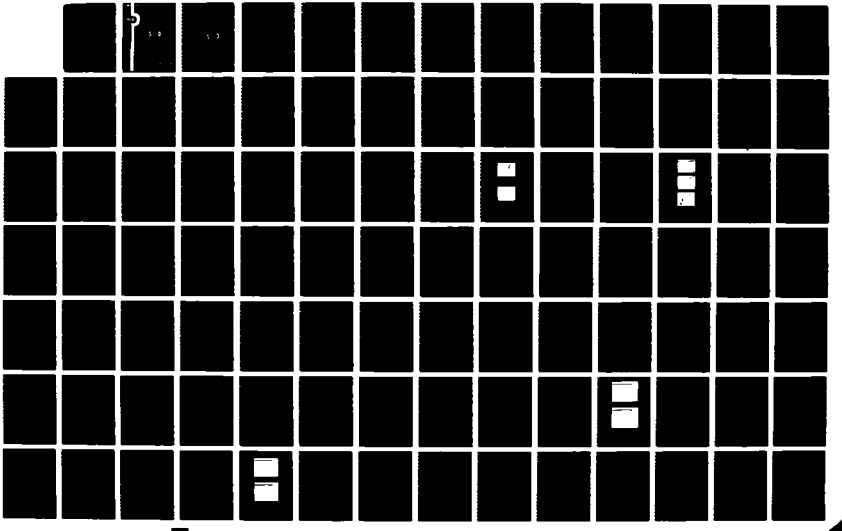

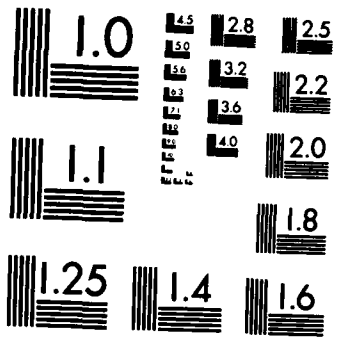

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
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The following report describes the results of research on III-V molecular beam epitaxial (MBE) growth, material characterization and the fabrication of heterostructure bipolar transistors (HBT) for very-high-speed logic applications. Work on the InGaP/GaAs heterojunction (HJ) was completed. Isotype HJs were grown and evaluated by a CV reconstruction method in order to determine the energy band offsets. It was found that $\Delta Ec = 0.22$ eV and $\Delta Ev = 0.24$ eV for the lattice matched composition. An inverted AlGaAs/GaAs HBT was investigated, and it was shown that an undoped, graded region between emitter and base would eliminate the conduction band spike and provide a buffer for Be diffusion. A new direction toward improvement in performance and fabrication techniques for the AlGaAs/GaAs HBT was successfully demonstrated. Graded-bandgap nonalloyed ohmic contacts using n+ InAs for the AlGaAs emitter and p+ GaSb for the GaAs base were provided by selective epitaxial regrowth. The MBE growth conditions for grading from GaAs to InAs and GaAs to GaSb were determined. Low specific contact resistances were observed for both contact types. A self-aligned AlGaAs/GaAs HBT with graded-gap contacts to both base and emitter was demonstrated.

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Final Report -- AFOSR-82-C-0344

Development of a Planar Heterojunction Bipolar Transistor for Very High Speed Logic

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ABSTRACT

The following report describes the results of research on III-V molecular beam epitaxial (MBE) growth, material characterization and the fabrication of heterostructure bipolar transistors (HBT) for very-high-speed logic applications. Work on the InGaP/GaAs heterojunction (HJ) was completed. Isotype HJs were grown and evaluated by a CV reconstruction method in order to determine the energy band offsets. It was found that ΔE_c = 0.22 eV and ΔE_v = 0.24 eV for the lattice matched composition. An inverted AlGaAs/GaAs HBT was investigated, and it was shown that an undoped, graded region between emitter and base would eliminate the conduction band spike and provide a buffer for Be diffusion. A new direction toward improvement in performance and fabrication techniques for the AlGaAs/GaAs HBT was successfully demonstrated. Graded-bandgap nonalloyed ohmic contacts using n+ InAs for the AlGaAs emitter and p+ GaSb for the GaAs base were provided by selective epitaxial regrowth. The MBE growth conditions for grading from GaAs to InAs and GaAs to GaSb were determined. Low specific contact resistances were observed for both contact types. A self-aligned AlGaAs/GaAs HBT with graded-gap contacts to both base and emitter was demonstated.

1. INTRODUCTION

The report which follows represents a summary of the important accomplishments of the project entitled "Development of a Planar Heterojunction Bipolar Transistor for Very High Speed Logic" funded under AFOSR contract 82-0344. Work was performed on this program over the interval from October 1, 1982 to June 30, 1987. The goals of this project were to investigate innovations in the design and fabrication of planar heterostructure bipolar transistors which would lead to high performance digital IC applications.

1.1 Objectives and Accomplishments

At the beginning of this program, predictions were made of the energy band lineup in the N-InGaP/p-GaAs system which indicated that the valence band offset would be greater than that obtained with the more familiar N-AlGaAs/p-GaAs system. A higher valence band offset would lead to a higher hole barrier between the narrow-gap base and wide-gap emitter, which in turn permits the use of base-to-emitter doping ratios much greater than 10. The high base doping is desirable for reducing the base access resistance and therefore increasing f_{max}. Lattice matching is possible in this system only over a very narrow composition range. At this composition, the InGaP has an energy gap of 1.87eV as compared with the 1.53eV for GaAs. Therefore, efforts were begun to investigate the MBE growth of InGaP on GaAs.

This work succeeded in growing several layers by MBE which were nearly lattice matched over a portion of the wafer surface. N-n and P-p isotype heterojunctions were grown to evaluate the conduction and valence band offsets respectively by C-V methods [1]. The results of this effort represented the first accurate measurement of this kind in this material system showing that ΔE_C = 0.22eV (0.48 ΔE_C) and ΔE_V = 0.24eV (0.52 ΔEg) [2,3].

While this result was close to the original predictions, it was found that the MBE growth method is not particularly well suited for this material system. The congruent sublimation temperatures for InP and GaP differ by about 200°C making the choice of a suitable substrate temperature a compromise at best. High P_2 fluxes were required to keep

the growing surface phosphorus stable. Finally, the uniformity of deposition and flux rate reproducibility in the MBE 360 system were not adequate to obtain dependable lattice matching and low defect densities needed for HBT fabrication. Although some successful preliminary device results were obtained [4], work was discontinued on this material because of the difficulties in MBE growth (as compared with MOCVD which seems to have relatively little difficulty). Even more importantly, while the work might have been continued if the reward seemed great, the discovery in 1984 that the valence band offset in the AlGaAs/GaAs system was larger than originally believed [5] eliminated any motivation to pursue InGaP/GaAs for the HBT. However, an unexpected consequence of our offset measurements is that the InGaP/AlGaAs system now looks quite interesting for optoelectronic device applications.

An AlGaAs/GaAs inverted HBT was also developed under the support of this project. The inverted structure is preferred over the more conventional emitter-up design because the high frequency performance will be enhanced through reduction in collector capacitance. Fabrication of such devices is more difficult, however, because the external base junction must be maintained in the wide gap material. Efforts were made to confine the injection to the area under the collector by ion implanting Be around the collector region, through the base, and into the emitter, forming a wide gap N-P junction in the external base area. Significant improvement in the design of the required graded region between the N-AlGaAs and p-GaAs was found to result through the use of an undoped graded-bandgap transition layer to eliminate the spike in the conduction band and provide a buffer to Be diffusion. Inverted N-p heterostructures were investigated experimentally to determine the optimum structure and growth approach to improve emitter injection efficiency at low current densities.[6] Further activity was determined to be unnecessary due to the very rapid progress being made on GaAs/AlGaAs HBT's for digital and analog circuits in industrial laboratories.

Finally, a completely new direction for obtaining ohmic contacts with the required low series resistance for HBT applications was investigated. Since the contacts to the device are highly critical in achieving the theoretical performance of the HBT, an alternative to the Au/Ge/Ni and Au/Zn "ohmic" alloyed contact systems has been evaluated. Following the earlier predictions of Woodall and Chang [7,8], the effectiveness of heavily-doped, graded-bandgap regions was explored for nonalloyed contacts. It is well known

that the Fermi level in n-InAs is pinned inside the InAs conduction band. Not as well known is the similar property for p-GaSb. The application of graded regions to semiconductors with no energy barrier for electrons (n^+ InAs) or for holes (p^+ GaSb) will lead to a reduction in series resistance when compared with the usual tunnel injection type of contact. In addition, nonalloyed contacts do not penetrate through the surface of the thin emitter and base layers. Consequently, thinner layers can be used, resulting in more reduction in series resistance, particularly for the emitter. Finally, the same metallization can be used for both emitter and base contacts, which lends itself nicely to self-alignment processes. Specific contact resistances below 3×10^{-7} Ω-cm^2 were observed on n-type transitions and 3×10^{-6} Ω-cm^2 on p-type transitions.

As a result of this work, the first HBT was grown and demonstrated which incorporated both graded-gap n and p type contacts on the same device [9,10]. The emitter was graded from n-AlGaAs to n^+ InAs. Then, after the emitter mesa was etched and masked, a second MBE deposition of p^+ GaAs to p^+ GaSb was grown, demonstrating that selective regrowth is possible on GaAs for p-type interfaces.

This first successful graded-gap HBT work led to a number of other reports of graded-gap emitters, where similar structures were effectively implemented for high performance HBT's [11,12]. No other devices have yet been reported with both graded base and emitter contacts.

Finally, self-aligned device fabrication methods were employed in order to improve the high frequency performance by reducing the parasitic base resistance and to eliminate the need for separate metal depositions for base and emitter contacts. Devices were obtained for which the simulated $f_{max} = 17$ GHz and $f_T = 37$ GHz.

1.2 Personnel and Publications

The program was administered by Prof. Stephen I. Long and Prof. Herbert Kroemer as co-principal investigators. The following students were employed as research assistants while working on this program and received their M.S. and Ph.D. degrees as indicated.

J. Blokker	M.S.	1983
B. Hancock	Ph.D.	1985
M.A. Rao	M.S.	1986

M.A. Rao Ph.D. expected 1987.

The following M.S. and Ph.D. dissertations were completed as a result of the support of this program:

B. Hancock, Ph. D. "Development of Inverted (Al,Ga)As Heterojunction Bipolar Transistors by MBE'

M. Rao, M.S. "Molecular Beam Epitaxial Growth and Energy Band Lineup Determination of (Ga,In)P/GaAs Heterostructures"

M. Rao, Ph.D. "AlGaAs/GaAs Heterostructure Bipolar Transistor with Non-Alloyed Graded-Gap Ohmic Contacts to the Base and Emitter" (in preparation)

The following presentations and journal publications resulted from this sponsorship:

M.A. Rao et al.,"Determination of Valence and Conduction Band Discontinuities at the (Ga,In)P/GaAs Heterojunction by C-V Profiling," *J. Appl.Phys.*, **61**: 643-649 (1987)

M.J. Mondry and H. Kroemer, "Heterojunction Bipolar transistor using a (Ga,In)P emitter on a GaAs base, Grown by Molecular Beam Epitaxy," *IEEE Elect. Dev. Lett.*, **EDL-6**: 175-177 (1985)

M.A. Rao et al., "AlGaAs/GaAs Heterostructure Bipolar Transistor with Non-Alloyed Graded-Gap Ohmic Contacts to the Base and Emitter," 44th IEEE Device Research Conference, Amherst, MA., 1986.

M.A. Rao et al., "An (Al,Ga)As/GaAs Heterostructure Bipolar Transistor with Non-Alloyed Graded-Gap Ohmic Contacts to the Base and Emitter," *IEEE Elect Dev. Lett.*, **EDL-8:** 30-32 (1987).

M.A. Rao et al., "A Self-Aligned AlGaAs/GaAs Heterostructure Bipolar Transistor with Non-Alloyed Graded-Gap Ohmic Contacts to the Base and Emitter," 11th Biennial Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Aug. 1987.

Preprints and reprints of these are attached as an appendix to this report.

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2. INVERTED HETEROSTRUCTURE BIPOLAR TRANSISTORS

2.1 The Inverted Structure

Recently, it was proposed [1] to build inverted heterojunction transistors, as shown in Fig. 2.1, where the emitter is now on the substrate side. This has several advantages. First, it is much more conducive to the construction of common emitter circuits, such as emitter coupled logic. For discrete devices, the use of the substrate as the emitter contact will greatly reduce the series resistance and inductance. This is important because the emitter is a low impedance node. Second, because the collector area is now a smaller fraction of the total device area, the collector capacitance will be reduced. Again, this is important because the collector is a *high* impedance node. In turn the emitter capacitance will be increased, but because of the relative impedances, the trade is beneficial.

The reduction of collector area is not without a cost. Any injection into portions of the base not covered by the collector will be lost as base current. Unless corrective measures are taken, the alpha will be at most equal to the ratio of collector area to emitter-base area. It is therefore necessary to reduce the current injected into the area under the base contacts. Two related techniques are available to do this. First, we may simply increase the p-type doping in the contact region, increasing the total charge (Gummel number) in this part of the base and proportionately decreasing the current injected. This may be seen from the Gummel-Poon relation [2]

$$J = \frac{qD_n n_i^2 e^{qV/kT}}{\int p\, dx} \qquad (2.1.1)$$

Additionally, this will improve the base contact and series resistances.

The second and more powerful technique is to extend the p-type doping into the wide-gap material, creating a wide-gap p-n junction. This is illustrated in Fig. 2.2. Now, at any given forward bias, the barrier height for injection of electrons will be larger in the contact region than in the active region, and the unwanted current will be suppressed by $e^{-\Delta E_g/kT}$.

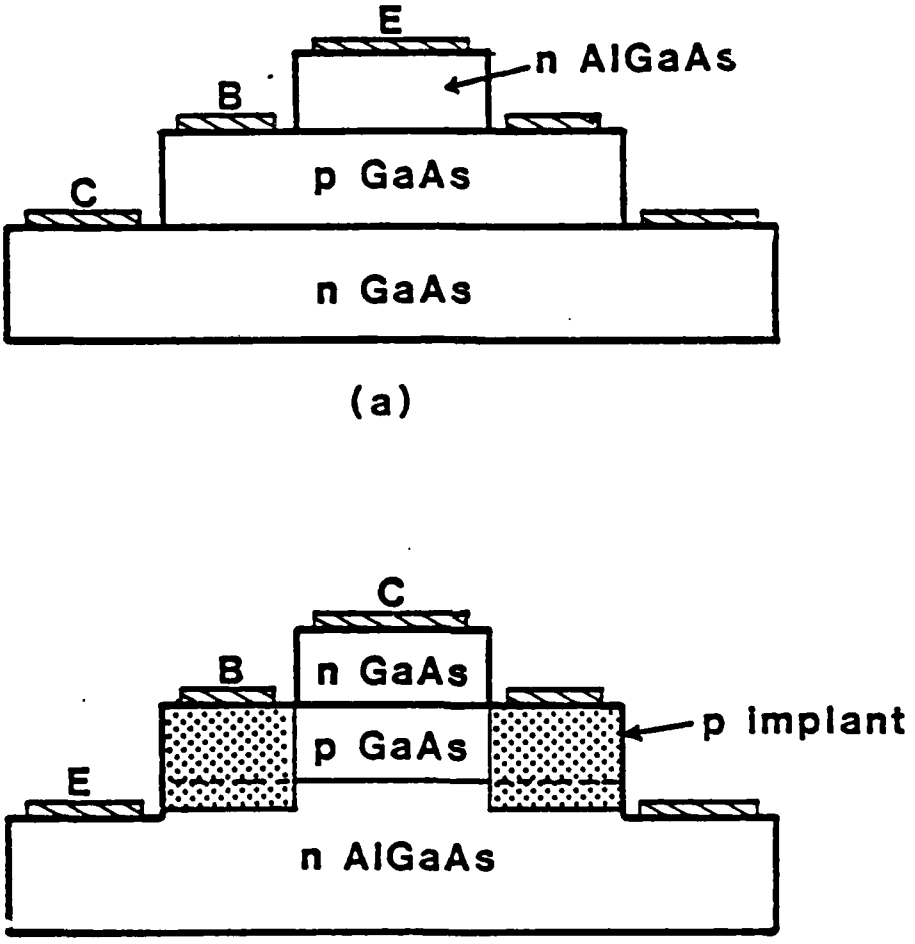


Fig. 2.1 Basic structures for (a) conventional, and (b) inverted heterojunction transistors.

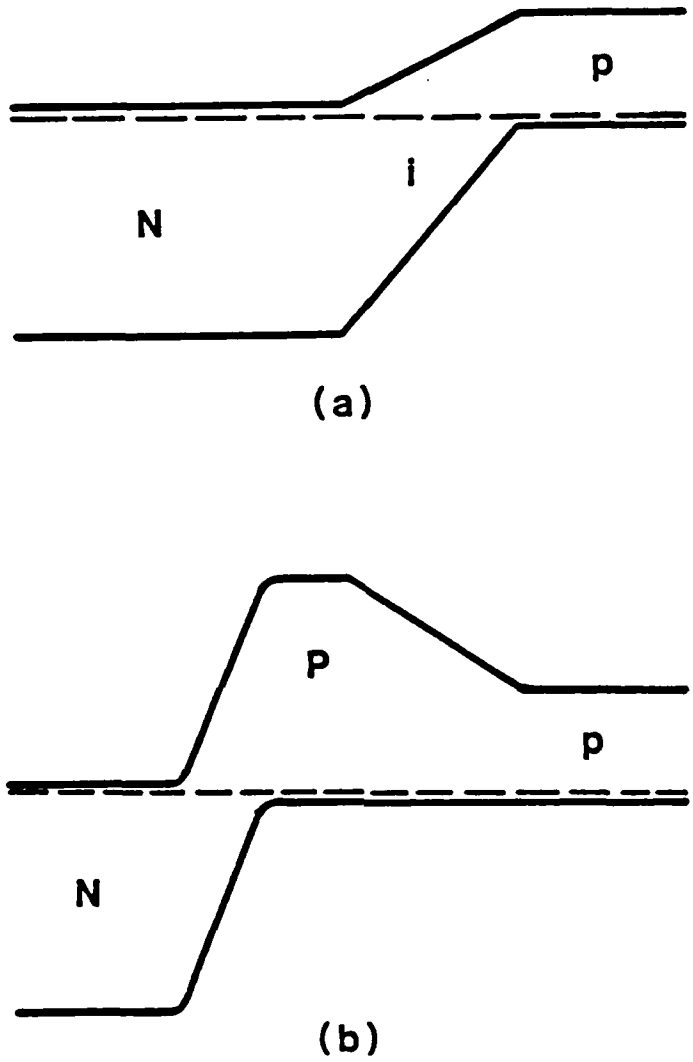


Fig. 2.2 Band diagrams illustrating (a) injecting emitter, and (b) blocking of the injection by extending the p-type doping into the wide-gap material.

The Gunnel-Poon relation points out that injection is a process controlled by the applied voltage and the characteristics of the *receiving* side of the junction. In the conventional bipolar transistor, the heavy doping of the emitter does not improve the injection efficiency by increasing the injection into the base; rather it reduces the back-injection into the emitter. Similarly, the more heavily doped the base, the lower will be the forward injection at any given voltage. If there are other competing current mechanisms, the lowered forward injection resulting from heavy base doping may cause a reduced current gain.

2.2 Graded Interfaces

Fig. 2.3 shows the band diagram for an abrupt N-p^+ junction. It is seen that the "spike" that forms increases the barrier height for injection of electrons, undoing part of the wide-gap emitter effect. In the limit of very high p-type doping the difference in electron and hole barrier heights will be reduced from ΔE_g to ΔE_v. The long-believed lineup rule [3] $\Delta E_c = 0.85\Delta E_g$ would make the problem quite severe. More recent measurements [4,5] find $\Delta E_c = 0.62\Delta E_g$. This is better, but still worth corrective action. The solution usually proposed is to grade the composition in order to eliminate the spike. Most experimental authors treat this grading rather cavalierly, but it deserves some detailed discussion.

Let us consider the construction of band diagrams for graded structures, beginning with some fundamentals of band lineups. If we assume that band lineups are transitive, as most theories do [6], then we might first define some arbitrary reference material (say, GaAs). Then, for any other material, we could measure the energy, χ, of the conduction band relative to the conduction band of the reference material. To determine the conduction band lineup between any two materials it is only necessary to subtract their respective χ values. Note that if we chose vacuum as the reference material we would obtain the Electron Affinity Rule [7]. Although there is evidence that the Electron Affinity Rule does not predict band lineups well [8] (suggesting a lack of transitivity for this rather drastic heterojunction), it is important to note that the formal description is the same.

The first step in drawing the band diagram is to draw the bands in the absence of any net electric charges or fields, the so-called intrinsic band diagram, based on the band

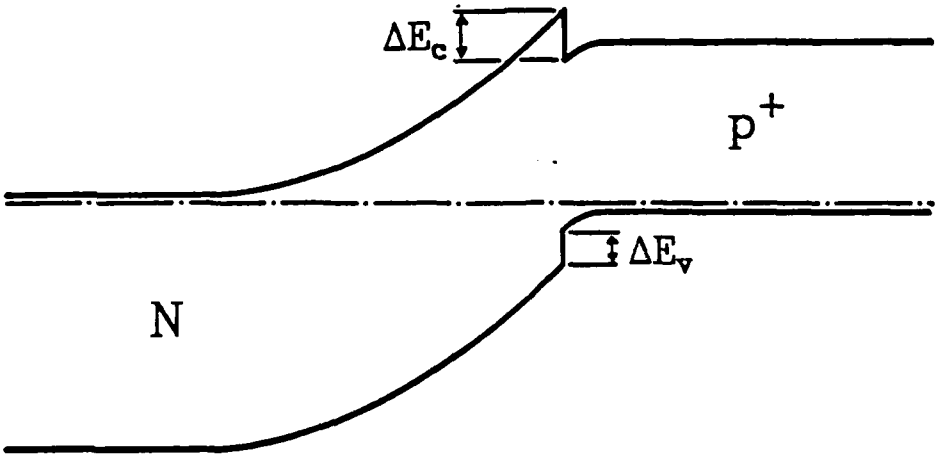


Fig. 2.3 Band diagram for an abrupt N-p^+ heterojunction.

positions discussed above. An example is shown in Fig. 2.4a for a linearly graded (Al,Ga)As junction. Note in this example the gradients in the conduction and valence bands. These gradients (in opposite directions!) are not true electric fields. They nevertheless exert real forces on the free carriers, and are called quasielectric fields.

Fig. 2.4b shows the ultimate band diagram we would like to achieve, with the inclusion of the true electrostatic potential. The electrostatic potential necessary to obtain this result is shown in Fig. 2.4c. It is the result of real net charge densities, i.e. the sum of ionized impurities and free carriers. This charge density distribution, shown in Fig. 2.4d, may be obtained by doping the ungraded regions heavily, while leaving the graded region undoped. Thin depletion regions will form, creating the sheets of charge which produce the desired uniform electric fields. The growth of such undoped layers is a simple matter by molecular beam epitaxy.

In the structure we have developed in this discussion the spike has been eliminated. Furthermore, the depletion width is now equal to the width of the undoped layer, nearly independent of bias. We may therefore make the emitter doping as large as we desire without sacrificing emitter capacitance.

This undoped graded structure, which we originally proposed in our contract renewal proposal [9] was also described later by Hayes *et al.* [10]

2.3 Other Undoped Structures

These concepts may be extended to further structures. In the case of the abrupt N-p^+ junction, the problem occurs because the band bending in the p-type material is small. This causes the spike to extend above the conduction band in the p-type material, raising the barrier height. If we grow an undoped layer on the narrow-gap side we may obtain an electrostatic potential drop which lowers the peak of the spike, as shown in Fig. 2.5. The injecting barrier is not raised by the spike, and the higher conductivity of the p^+ material is maintained. This approach does not require the growth of graded material. We believe that this structure will be very useful for heterojunction devices. It is not clear whether the notch formed by the conduction band discontinuity would harm high frequency operation.

Undoped layers are also useful for the collector-base depletion region. This allows a

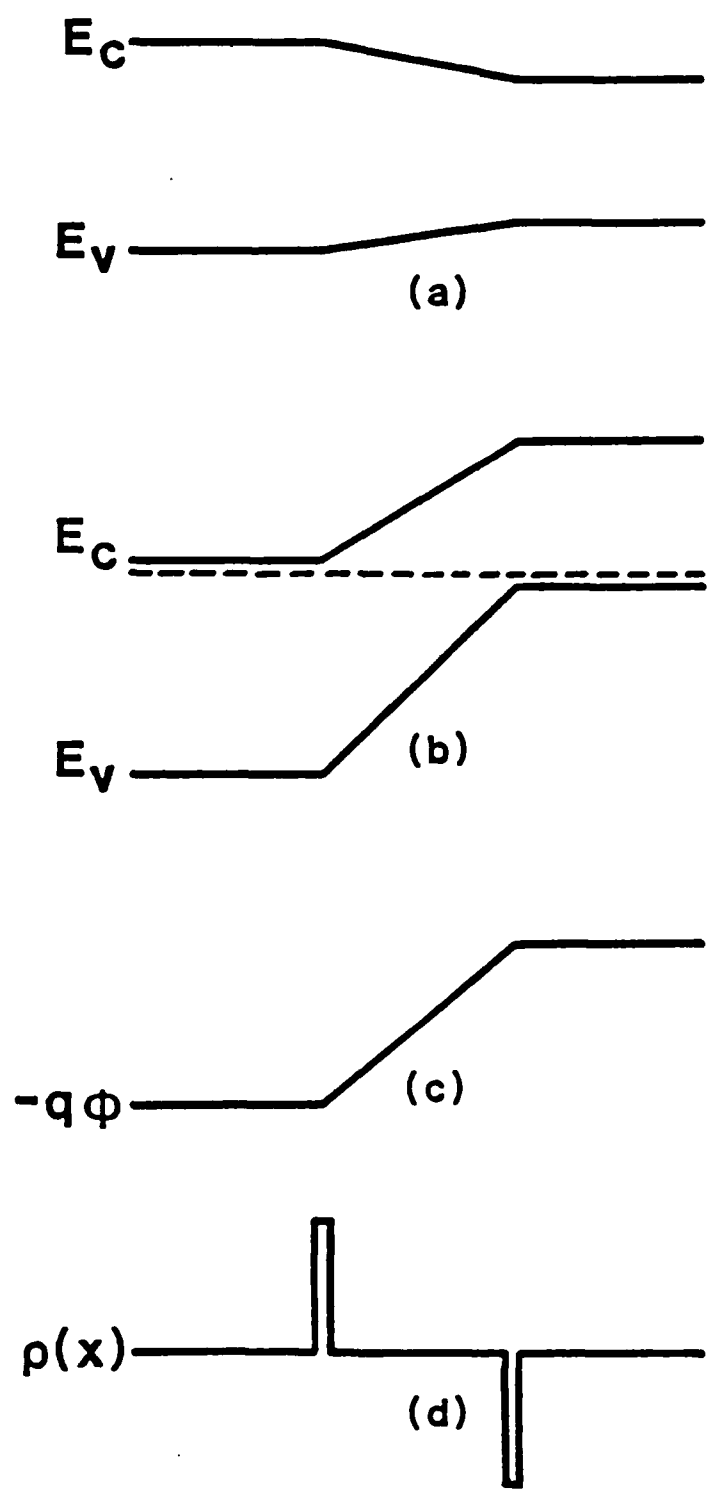


Fig. 2.4 Development of the band diagram for a graded emitter. (a) Intrinsic band diagram. (b) Desired final band diagram. (c) Electrostatic potential. (d) Net charge distribution.

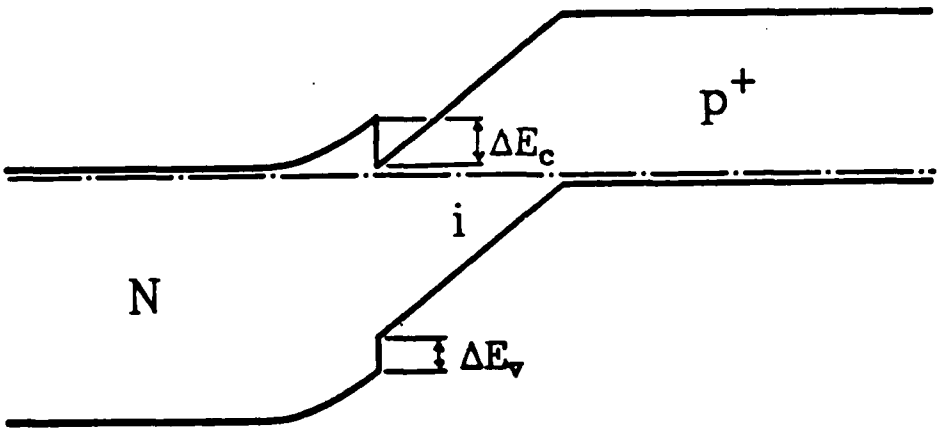


Fig. 2.5 Band diagram for an N-i-p^+ heterojunction.

relatively high breakdown voltage for a given depletion width because the electric field has its maximum value across the full width. Again, the capacitance is nearly independent of the bias.

2.4 Experimental

2.4.1 MBE Growth

All layers were grown in a Varian MBE 360 system on (001) oriented n^+ GaAs. Substrates were prepared by conventional techniques: i.e., solvent cleaning; etching in 1 H_2O_2:4 NH_4OH:20 H_2O; dilution of the etch with deionized water for 5 minutes to grow a passivating oxide; and, finally, mounting on the molybdenum block with molten indium. On loading into the growth chamber from the load lock, the substrates were heated to 350°C for approximately 30 minutes to desorb any gasses and allow the system pressure to drop. We have found that this greatly reduced the number of oval defects, to about $1000/cm^2$. The oxide was then desorbed by heating to 650°C in the presence of the background arsenic vapor only. When a clear gallium stable reconstruction was observed by Reflection High Energy Diffraction (RHEED) the growth was begun.

Elemental sources of gallium and aluminum were used. Arsenic in the form of As_2 was produced by the thermal decomposition of polycrystalline GaAs. The arsenic furnace was capped with a relatively cool baffle which served to remove gallium from the beam. N-type and p-type dopants were silicon and beryllium, respectively, from elemental sources.

2.4.2 Device Fabrication

After removal from the MBE system, samples were demounted and the indium was etched from the backsides with warm HCl. During etching, the front surface was protected with wax. Next the backsides were lapped smooth with 5μm abrasive. This was necessary both for use in the mask aligner and for the formation of backside ohmic contacts. Although the mounting indium is generally reported to make ohmic contact to n-type substrates, we found it inadequate for use in quantitative measurements.

For transistor samples, the next step was the etching of the collector mesa through to

the base layer. It is necessary to do this with some accuracy in order to etch down to the relatively thin base layer without etching through it. We have found 1 H_2O_2:4 H_2SO_4:35 H_2O to be a very suitable etchant. This etchant must be cooled to room temperature before use since heat is liberated duing the mixing of the acid and water. The etch rate is measured to be 215nm/min, both for GaAs and for (Al,Ga)As, and is quite reproducible. As a precaution, each batch of etchant was tested first on a sliver of the wafer being processed. Point probes can also be used to determine whether the p-type layer has Cr:Au reached. The breakdown voltage for heavily doped p-type material is typically less than 2 volts, whereas the breakdown voltage for undoped material is much higher.

Ion implantation for transistors was performed using as a mask the photoresist used for etching the collector mesa. This results in a self aligned structure. The implantation hardens the photoresist, necessitating the use of an oxygen plasma for removal. This was followed by the annealing of the implant.

Next, the base mesa was etched well into the substrate using the same etchant. Backside contacts were evaporated Au:Sn. Although this metal does not exhibit as low a contact resistance as Au:Ge/Ni it is much more tolerant of annealing conditions. Because of the large area the total contact resistance is sufficiently low. Annealing of Au:Sn was done for 2 minutes at 450°C in a forming gas atmosphere (85% N_2:15% H_2). Au:Zn or Cr/Au:Zn was deposited on the collector and also on the emitter (redundant with the backside contact). These can also be used for preliminary testing without annealing since the collector acts as a current source. Both types of contacts were generally annealed for 2 minutes at 450°C.

As a dielectric layer we have used photoresist, hard baked for 30 minutes at 180°C. This dielectric is the simplest to deposit and pattern. The hard bake not only renders the photoresist impervious to solvents, but also causes it to flow into a tapered edge, ideal for step coverage. Finally a layer of Cr:Au was deposited as the interconnect metal.

Processing of diodes was roughly similar. After the backside lapping any ion implantation and annealing was done. Au:Sn was deposited on the back and annealed. Au:Zn or Cr/Au:Zn was lifted off, and finally, the mesas were etched. Again, it was found desirable to be able to make some measurements before annealing the contacts.

2.5 p-N Junction Experiments

Preliminary attempts at making inverted transistors yielded devices with negligibly low current gains. It was concluded that the fastest way to converge on a working device was to concentrate on the emitter base junction. To this end we fabricated a variety of junction structures to test their suitability for use as emitters. The fabrication of these devices is quicker and more reliable than that of transistors.

In order to find a good emitter, six structures were tried. All had several features in common. The n-type layer, 100nm thick, was grown on the substrate side and was silicon doped approximately $5 \cdot 10^{17}$ cm^{-3}. To minimize any series drops, a graded layer of approximately 50nm was grown between the GaAs substrate and the (Al,Ga)As emitter. The p-type layer wa doped $2 \cdot 10^{18}$ cm^{-3} and was 250nm thick. The structures are listed in Table I and the expected band diagrams are shown in Fig. 2.6. The measured log J-V curves are shown in Fig. 2.7.

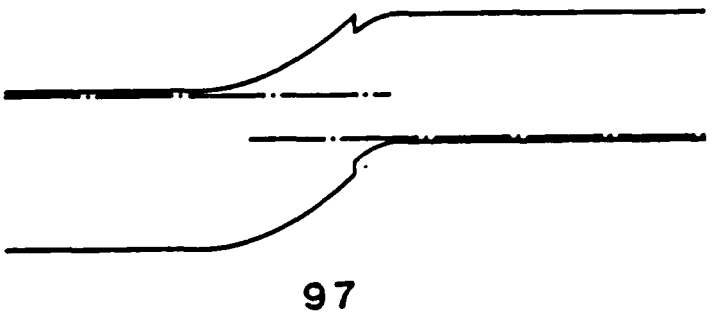
The first structure, layer 97, is an abrupt heterojunction. Its ideality factor is near 2. The large current compared to the other devices rules out the possibility of a series voltage drop as responsible, since all should have roughly the same level of injection current. It was found that the current scales very closely with area, so we conclude that the current is carried primarily by depletion region recombination. This is not useful for an emitter.

Because of the large depletion layer recombination we concluded that the density of recombination centers in the (Al,Ga)As was high. (Al,Ga)As grown by MBE is known to deteriorate in quality as the layer becomes thicker. This is a special handicap to the inverted structure transistor. We therefore decided that it would be useful to move the location where n=p into the better-quality GaAs. This was done for layer 98 by growing a 50nm undoped GaAs layer between the (Al,Ga)As and the p-GaAs. As seen from the J-V curves and the ideality factor, this improved the device performance. This spacer layer, included in all subsequent structures, served two additional purposes. First, it provides some latitude for possible diffusion of beryllium. This diffusion, if it crossed the heterojunction, would convert the junction to a wide gap one, which would be undesirable. Second, the spacer will lower the peak of the conduction band spike below the base conduction band level.

Table I

Test Diode Structures

97:	250nm	$p=2\cdot10^{18}$	GaAs
	100nm	$n=5\cdot10^{17}$	AlGaAs
98:	250nm	$p=2\cdot10^{18}$	GaAs
	50nm	nid	GaAs
	100nm	$n=5\cdot10^{17}$	AlGaAs
99:	250nm	$p=2\cdot10^{18}$	GaAs
	50nm	nid	GaAs
	50nm	nid	Graded
	100nm	$n=5\cdot10^{17}$	AlGaAs
100:	250nm	$p=2\cdot10^{18}$	GaAs
	50nm	nid	GaAs
	15nm	nid	Digital Grade:
			1.5nm AlGaAs
			2.0nm GaAs
			3.0nm AlGaAs
			2.0nm GaAs
			4.5nm AlGaAs
	100nm	$n=5\cdot10^{17}$	AlGaAs
103:	250nm	$p=2\cdot10^{18}$	GaAs
	50nm	nid	GaAs
	100nm	$n=5\cdot10^{17}$	(15nm AlGaAs/1.5nm GaAs)



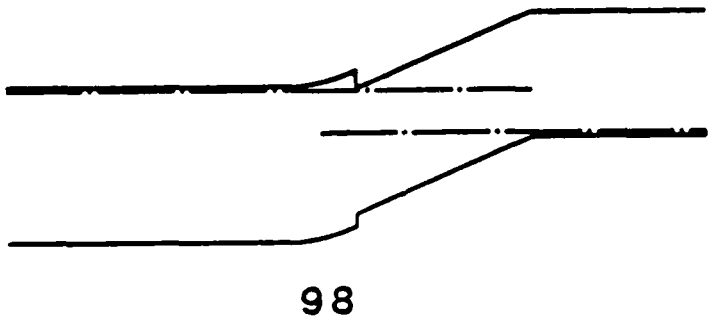
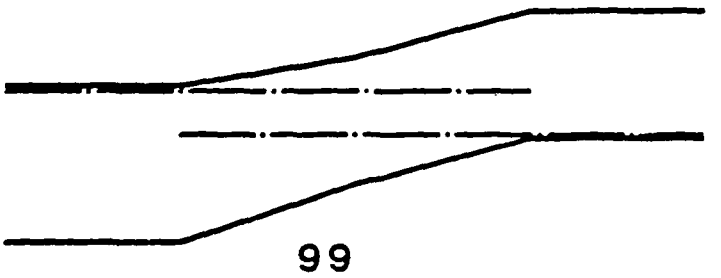
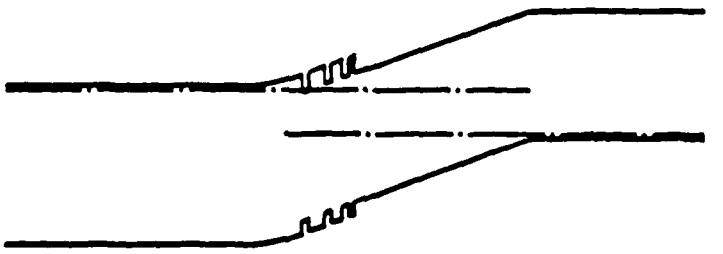


Fig. 2.6 Expected band diagrams for the test diodes listed in Table I.



99



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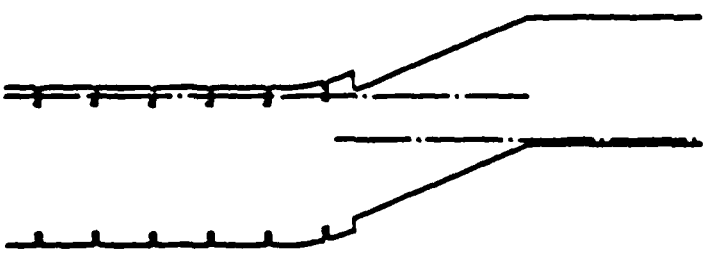


103

Fig. 2.6 (continued)

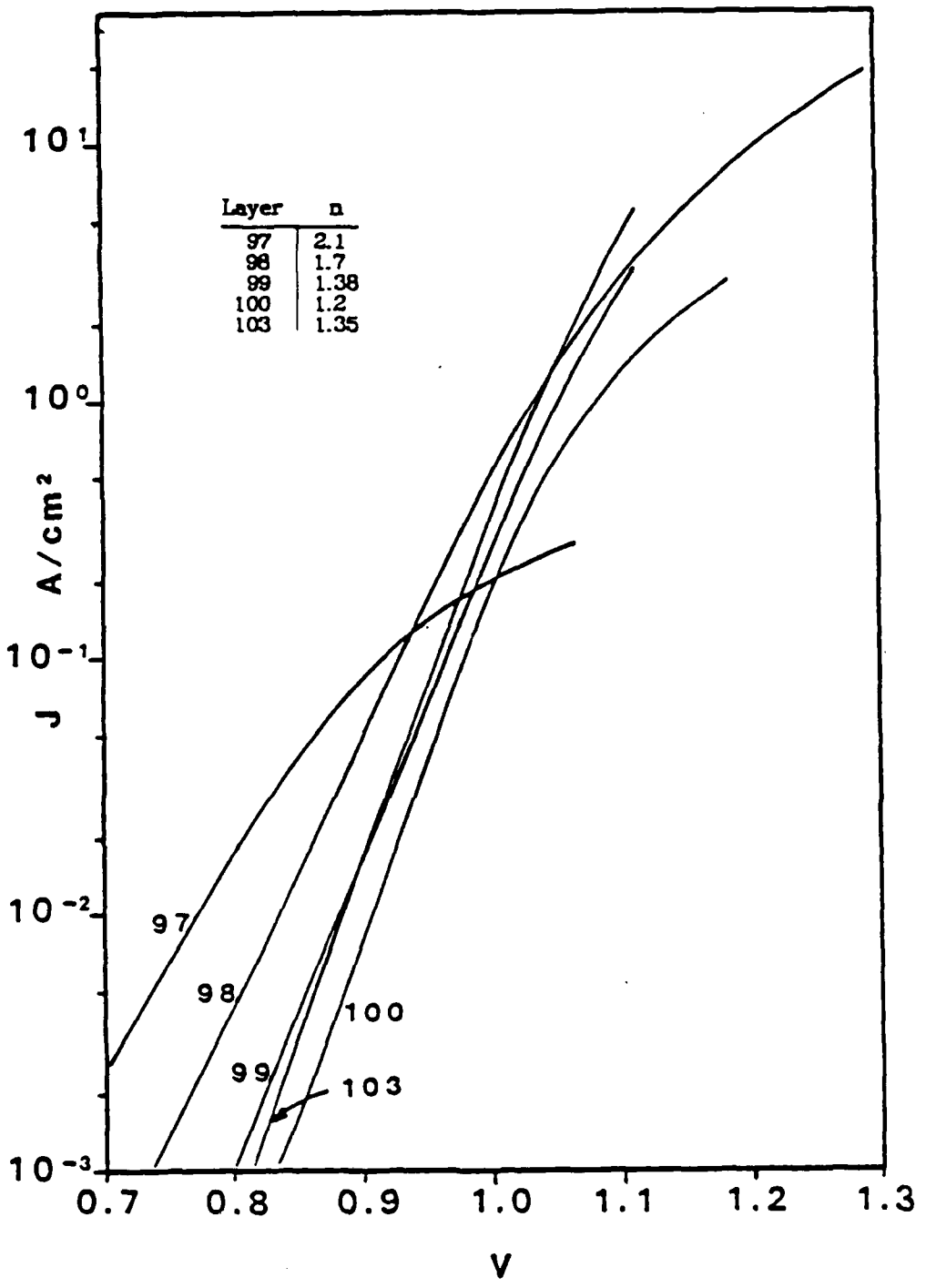


Fig. 2.7 Log J-V curves for diodes listed in Table I.

Layer 99 was grown with a 50nm undoped graded layer, followed by the undoped GaAs layer. The ideality factor and current are seen to be significantly improved.

Layer 100 was grown with an interface which was graded digitally, as proposed by Su *et al* [11]. This is expected to have two benefits. First, it should approximate a graded layer. Second, it has been found that the growth of a thin GaAs layer within an (Al,Ga)As layer improves the quality, presumably by trapping surface accumulating impurities. The I-V curves show the lowest current and ideality factor. It must be pointed out, however, that the current for these devices did not scale with the area. This was probably caused by erratic contacts which had different voltage drops for different devices. This would shift the curves in voltage, which has a similar effect as scaling the current.

Both layers 99 and 100 suggest that the quality of the growing (Al,Ga)As may be responsible for the poor junction characteristics. It has been found by Baba *et al.* [12] that the deep levels in (Al,Ga)As are produced by the coincidence of aluminum, gallium, and silicon. When they grew a superlattice where only the GaAs layers were doped they found no freeze out of carriers at low temperature. Layer 101 was grown using such a superlattice of (1.5nm AlAs/2.5nm GaAs:Si). The diodes fabricated on this layer showed no conduction up to 400 volts. It appeared that the superlattice layer was insulating.

In another attempt to grow better-quality material, layer 103 was grown with a "cleanup" superlattice, consisting of 1.5nm of GaAs interspersed into the silicon doped (Al,Ga)As every 16.5nm. The current scaled with the area for these devices. The low current and ideality factor show the high quality of this device, especially as compared to its counterpart, layer 98.

Barrier height measurements were made on layers 99, 100, and 103. For each of these, log J-V curves were plotted at four different temperatures. The barrier height was obtained from the slope of log J/T^3 *vs* $1/kT$ at various voltages. The higher voltages seemed to yield better results. Fig. 2.8 shows the results for layer 99. The measured barrier heights are:

99: 1.40 eV

100: 1.47 eV

103: 1.48 eV

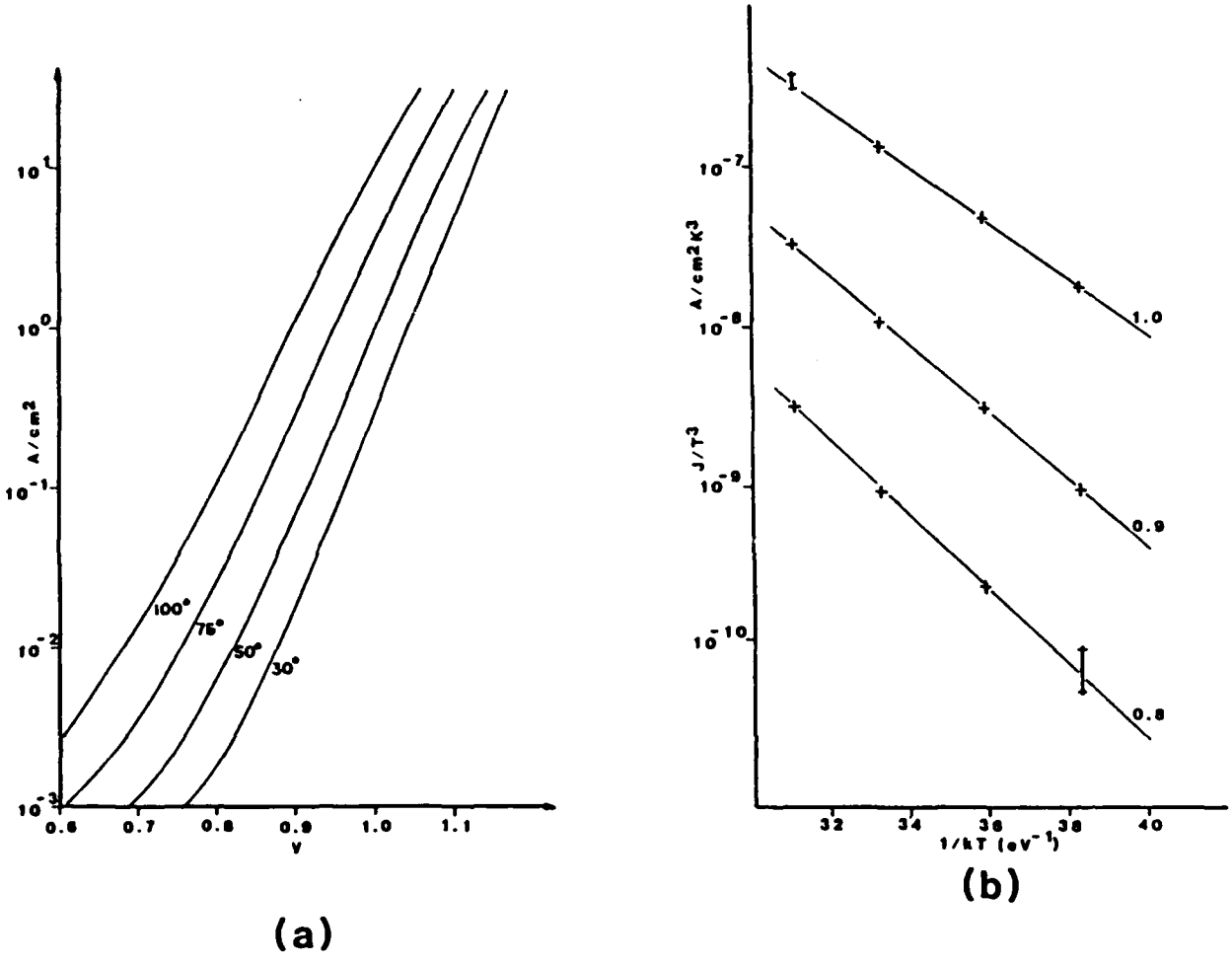


Fig. 2.8 Barrier height measurements on layer 99. (a) I-V measurements at 30°C, 50°C, 75°C, and 100°C. (b) Log (J/T^3) *vs* 1/kT for V = 0.8, 0.9, and 1.0 V.

This confirms that the junction has not been made wide gap by the diffusion of beryllium. These values are, in fact, somewhat low. The expected value is the bandgap of GaAs projected to 0 K, which is [13] 1.558 eV.

2.6. Transistor Wafers

2.6.1. Introduction

Transistors were fabricated on wafer 114. The layer is described in Table II, and the assumed band diagram is shown in Fig. 2.9.

Each reticle contained transistors of six different geometries and a variety of test structures. This work used the transistors designated Q1, Q2 and Q3. Some key parameters of the devices are:

	Q1	Q2	Q3
Collector-Base Junction			
	$20 \times 20\ \mu m^2$	$20 \times 100\ \mu m^2$	$150 \times 150\ \mu m^2$
	$=4 \cdot 10^{-6}\ cm^2$	$=2 \cdot 10^{-5}\ cm^2$	$=2.25 \cdot 10^{-4}\ cm^2$
Emitter-Base Junction			
	$68 \times 28\ \mu m^2$	$68 \times 108\ \mu m^2$	$198 \times 158\ \mu m^2$
	$=1.9 \cdot 10^{-5}\ cm^2$	$=7.3 \cdot 10^{-5}\ cm^2$	$=3.1 \cdot 10^{-4}\ cm^2$
A_{CB}/A_{EB}	0.21	0.27	0.72

Transistors Q4, Q5 and Q6 were designed for other purposes not applicable here. Each transistor had two base contacts on opposite sides of the collector. All base contacts were 20μm wide. Fig. 2.10 shows the geometry of a Q1 transistor.

The test structures included cross resistors for measuring sheet resistance [14], transmission line [15] and Kelvin bridge [16] structures for measuring contact resistance,

Table II

Transistor layer 114 structure

50nm	$n=2\cdot10^{18}$	GaAs
250nm	nid	GaAs
250nm	$p=2\cdot10^{18}$	GaAs
50nm	nid	GaAs
50nm	nid	Graded
500nm	$n=2\cdot10^{18}$	(15nm AlGaAs/1.5nm GaAs)
50nm	$n=2\cdot10^{18}$	Graded (15nm AlGaAs/1.5nm GaAs)
	$n=2\cdot10^{18}$	GaAs Substrate

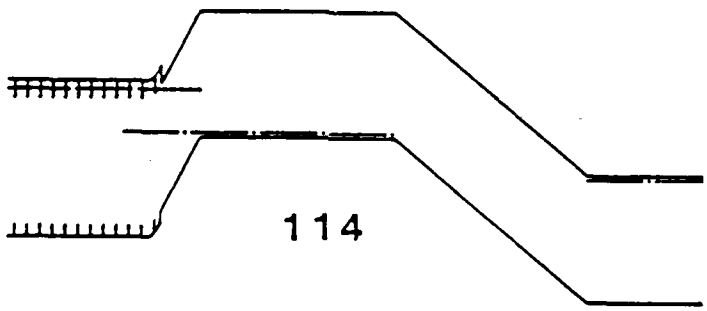


Fig. 2.9 Assumed band diagrams for the transistor on wafer 114.

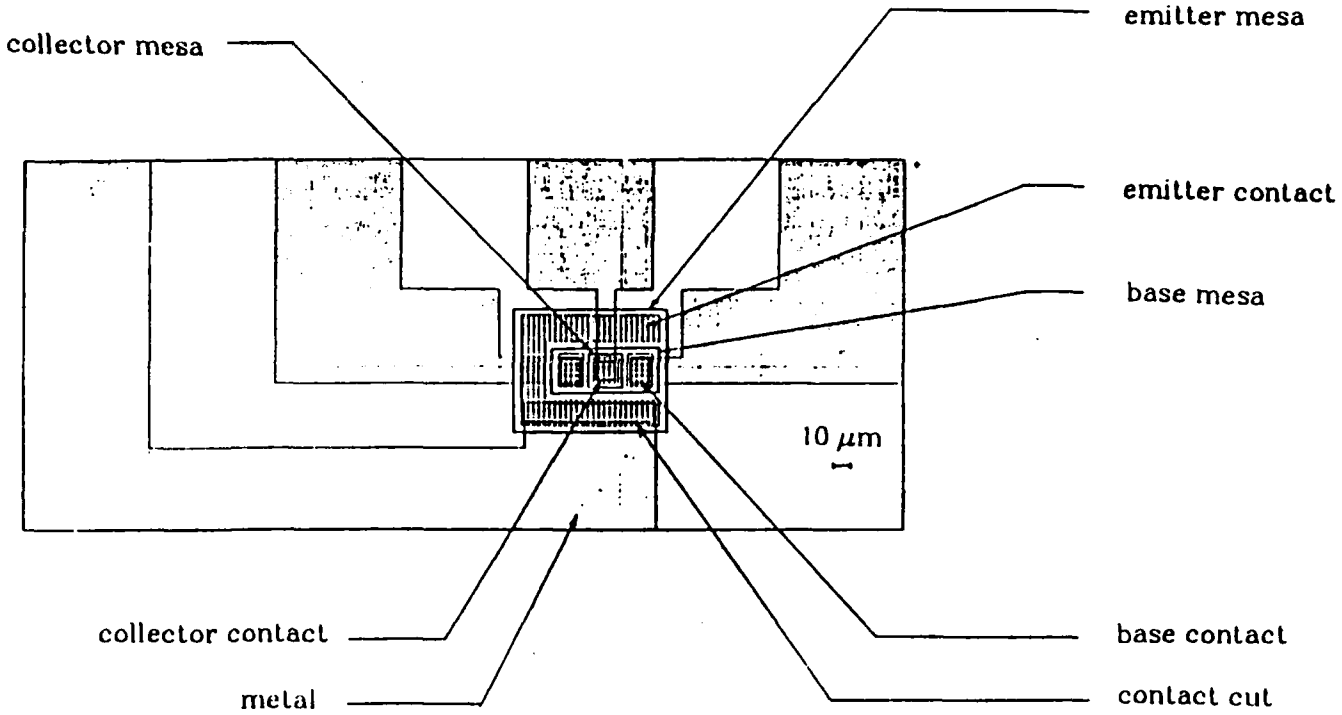


Fig. 2.10 The layout of the Q1 transistor.

and collector-less emitter-base diodes. This permitted us to measure the sheet resistance of the as-grown base layer, and also allowed us to characterize the unimplanted emitter-base junction.

Note that on wafer 114, the emitter layer was grown 0.5μm thick to prevent the implant from converting it entirely to p-type. To maintain the quality of such a thick (Al,Ga)As layer, a "cleanup superlattice" was used. This consisted of the repeated structure 1.5nm GaAs/15nm (Al,Ga)As. The ground state of the narrow well is only 65meV below the (Al,Ga)As conduction band and the wave function extends through the entire barrier. Both materials were doped heavily n-type, and it was hoped that this superlattice would behave essentially as the bulk alloy. The interface to the substrate was graded in the usual manner, i.e. the aluminum fraction in the (Al,Ga)As was increased linearly over 50nm while the superlattice period was held constant. At the emitter-base junction, the superlattice was terminated at the beginning of the undoped, graded layer.

In addition, the n-type doping was increased to $2 \cdot 10^{18}/cm^3$. This was the value originally intended for the earlier devices. The layer structure was otherwise unchanged.

In an attempt to improve the planarity of the devices and eliminate the critical etching step, the collector mesa was not etched down to the base layer. Instead, the implantation was performed at a higher energy, 160KeV at a dose of $4 \cdot 10^{14}/cm^2$. A second implant of $1 \cdot 10^{14}/cm^2$ at 50KeV was performed to make contact to the base through the undoped region (collector depletion layer). Prior to the implantation the wafer was cleaved into two parts: 114/1 which received both the shallow and deep implants, and 114/2 which received only the shallow implant. Wafer 114/2 served the same function as the reticles on wafers 105 and 106 which were masked from the implant with copper tape, i.e. as a control sample on which the external portion of the base was not converted to wide-gap.

After the implant, a collector mesa of 100nm was etched. This was done to remove the silicon doped layer at the surface, in case it had not been converted to p-type. This should also improve the collector breakdown characteristics by eliminating the lateral p^+-n^+ junction. The mesa was etched immediately after the implant, using the same photoresist mask. The etch rate was found to be unchanged. The implant was then furnace-annealed at 750°C for 15 minutes with As overpressure.

Immediately prior to loading into the evaporator for contact deposition the wafers were cleaned [17] by a 5 second dip in 1 NH_4OH : $10H_2O$. The contacts were annealed [18] for 120 seconds in a 490°C furnace with flowing N_2/H_2 with the wafers standing edgewise parallel to the flow in a slotted boat. The wafers were preheated to 100°C before being pushed to the hot zone of the furnace.

2.6.2 Test Structure Results

Both p-type and n-type contacts were ohmic. Kelvin bridge measurements indicated contact resistivities of about $10^{-4}\Omega cm^2$ for both types. This relatively high value probably resulted from the use of a three-point measurement technique, the large geometries, and the inaccuracies of the alignment. This number, which can be taken as an upper limit on the actual contact resistivity, represents a room temperature kT drop at a current density of 250 A/cm^2.

The cross-resistor measurements were noise-free and provided the following results:

collector	240 Ω/□
114/1 base	210 Ω/□
114/2 base	590 Ω/□
unimplanted base	1000 Ω/□

The base sheet-resistance measurements represent the implanted portions of the device. As described before, 114/2 received only the shallow implant, while 114/1 received both the shallow and the deep implants, a total dose five times as large. The sheet resistance of the unimplanted material was obtained from the resistance between opposite base contacts on a Q3 device.

2.6.3. Diode Results

Fig. 2.11 shows log J-V curves for the emitter-base diodes on wafers 114/1 and 114/2. Three sizes of diodes were used, corresponding to the three transistor emitter-base junctions, i.e. $1.9 \cdot 10^{-5}$, $7.3 \cdot 10^{-5}$, and $3.1 \cdot 10^{-4} cm^{-2}$.

Considering first the results for 114/2, which received only the shallow implant, we see that in the midrange the curves agree very well. At higher currents, the curves for the

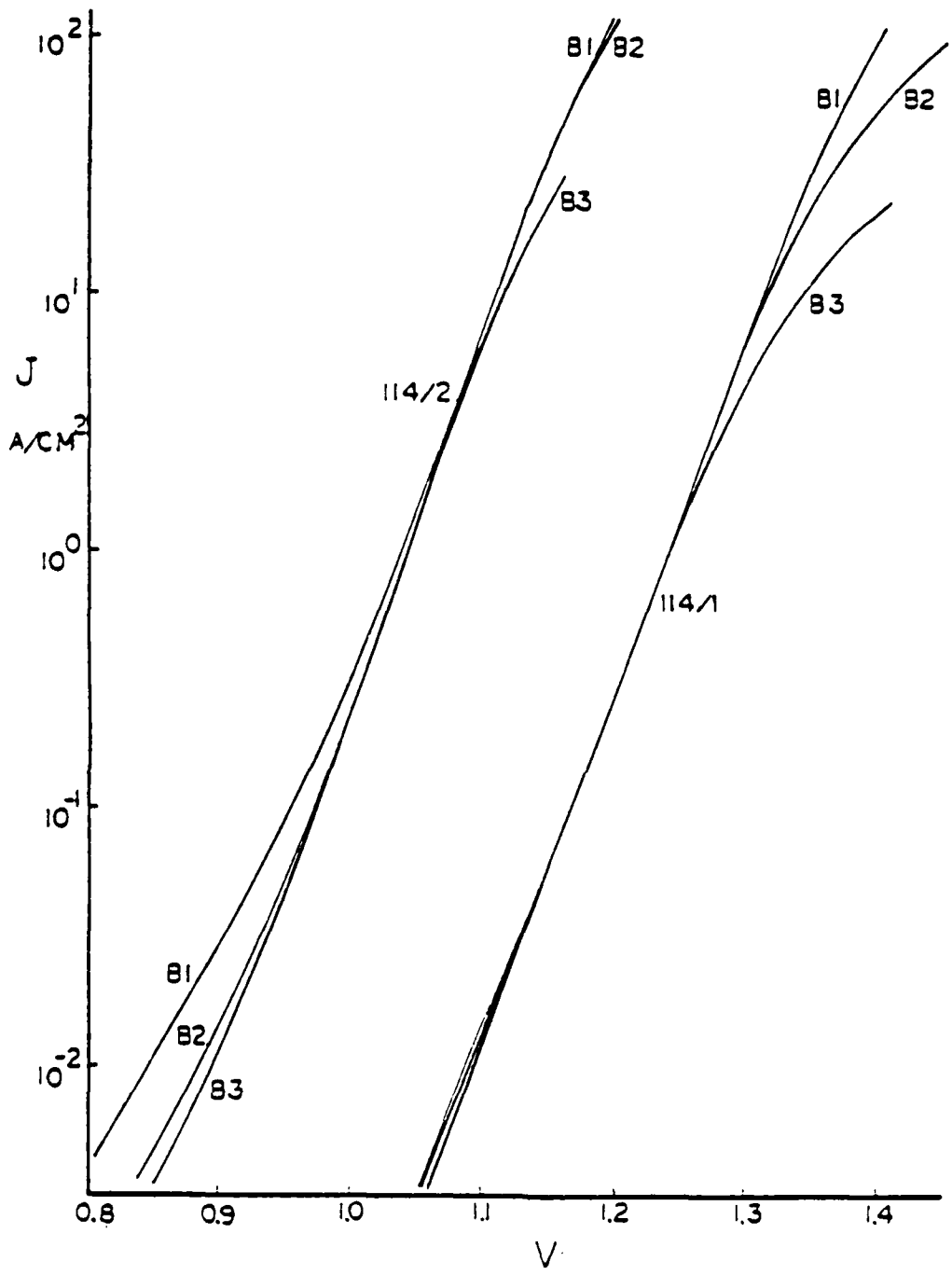


Fig. 2.11 J-V curves for emitter-base test diodes on wafers 114/1 and 114/2.

larger devices fall to the right of those for smaller devices. This is interpreted as an increase in the series voltage drop caused by a larger total current flowing through a series resistance which does not decrease with increasing device size. This resistance of around 5Ω is probably related to the probe station and wiring. At low currents the ideality factor increases to near 2. Now the curves for the smaller devices are above those for the larger ones. The recombination current does not scale with the area of the devices, but rather with the perimeter. We therefore identify the origin of this undesired current as perimeter recombination.

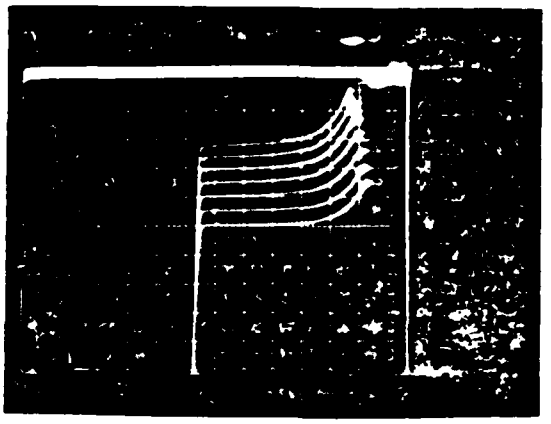
The curves for 114/2 lie far to the right of, or, equivalently, far below those for 114/1. The current scales very closely with the area and has an ideality factor of 1.2. Again we see the effect of a constant series resistance at high currents, but this time there is no sign of the perimeter recombination current at low levels.

I-V measurements were made as a function of temperature for both these devices. We extract energy gaps of 1.72eV for 114/1 and 1.46eV for 114/2. Althought both these values are lower than expected, the difference corresponds roughly to the composition of the (Al,Ga)As.

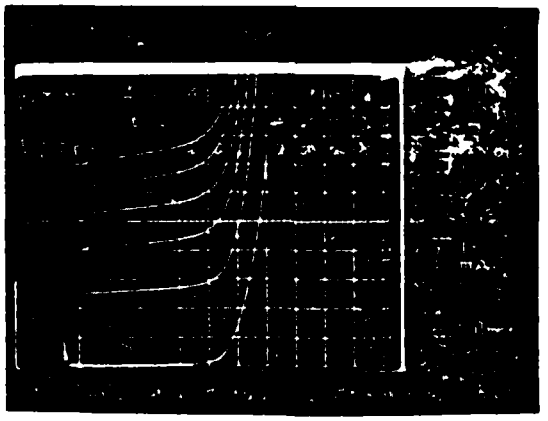
At 25°C this bandgap difference predicts that the *electron* injection should be reduced by a factor of $2 \cdot 10^4$. The current is, in fact, only reduced by a factor of 500, corresponding to a shift in turn-on voltage (including the ideality factor) of 0.2 volts. This suggests that the current is carried by back-injected holes. Note that the increase in the bandgap of the base goes entirely into raising the electron barrier, leaving the hole barrier unchanged. We conclude that a higher aluminum composition should be used.

2.6.4. Transistors

We begin with the results of wafer 114/2, since these are more easily understood. Fig. 2.12 shows common base and common emitter curves. Several features are evident. First, the alpha of 0.5 is lower than the area ratio of 0.72. Again, this may be the result of using only a single base contact. Second, the collector breakdown is not very sharp, although this is partly influenced by the low scale of the current. In the forward direction, the collector turn-on voltage is quite low, 0.6V. This is also reflected in the large common-



(a)



(b)

Fig. 2.12 (a) Common base curves for a Q3 transistor, and (b) common emitter curves for a Q2 transistor on wafer 114/2.

emitter saturation voltage. This saturation voltage is the difference between the normal turn-on voltage of the emitter-base junction and the abnormally low turn-on voltage of the collector-base junction , and is not caused by a spike at the emitter-base junction [19] or at the collector-base junction [20]. Fig. 2.13 shows logarithmic plots of the collector and base currents versus emitter-base voltage, with V_{cb}=0. This clarifies the situation. At low voltages the collector current has an ideality factor of 1, as is expected for injection. If the asymptote for this curve is compared with the n=1 asymptote for the emitter-base test diodes good agreement is found. At low voltages, the base current also has in ideality factor of 2. Comparing different size devices, it is found that this current scales with the device perimeter, so again we see perimeter recombination. This limits the alpha at low currents. This recombination current is much larger than the one associated with the emitter-base test diodes. The cause may be related to the mask edges on the transistor implant. The diodes, in contrast, were formed in an area which received a blanket implant, and were then defined by an etch.

At higher voltages, both collector and base currents are seen to increase in ideality factor, even beyond 2. This suggests that series resistance as well as crowding is significant. Current crowding limits the alpha at high currents, and the area ratio value is never reached.

Fig. 2.14 shows common base and common emitter curves for wafer 114/1. The collector-base characteristics are even worse than for 114/2. The beta for these devices reaches a value near 10. Fig 2.14c shows that at high currents there is a negative differential resistance.

We show logarithmic I-V plots in Fig. 2.15. At low voltages the collector current shows an n=1 behavior, again agreeing with the test diodes on 114/2. The base current shows an ideality factor of about 1.6 and is found to scale with the area. Temperature dependence measurements indicate bandgaps of 1.49eV for the collector current and 1.52eV for the base current.

The origin of the negative resistance is not clear, but its onset is apparent in the log I-V curves, in both the collector and base currents. In the negative resistance regime an

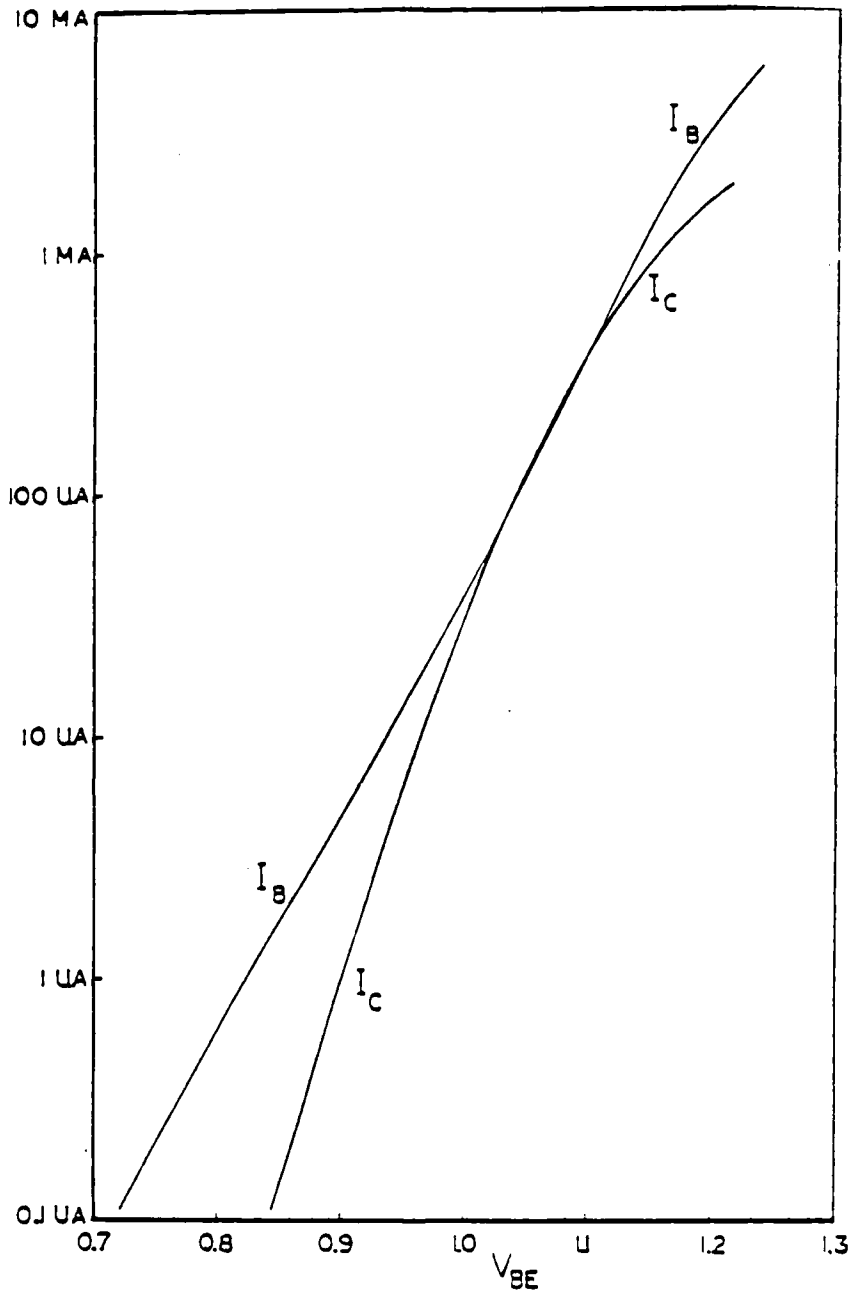
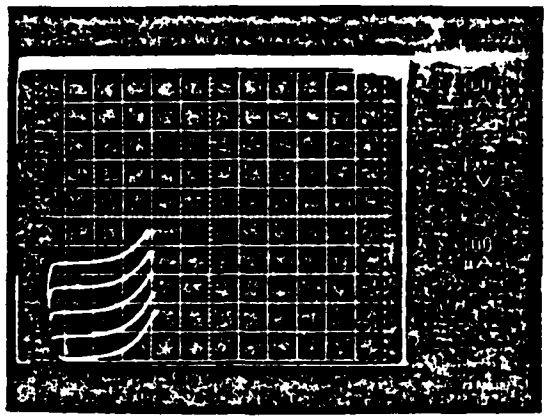
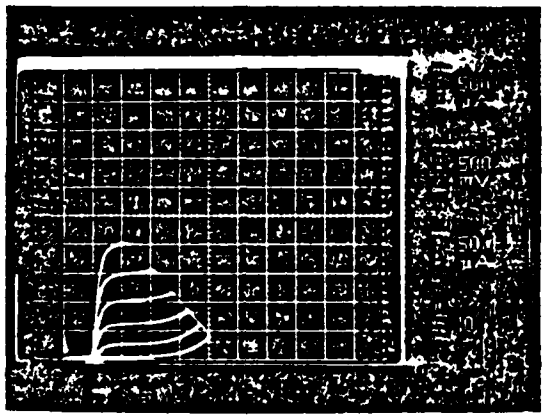


Fig. 2.13 Collector and base currents versus emitter-base voltage for a Q3 transistor on wafer 114/2.

(a)



(b)



(c)

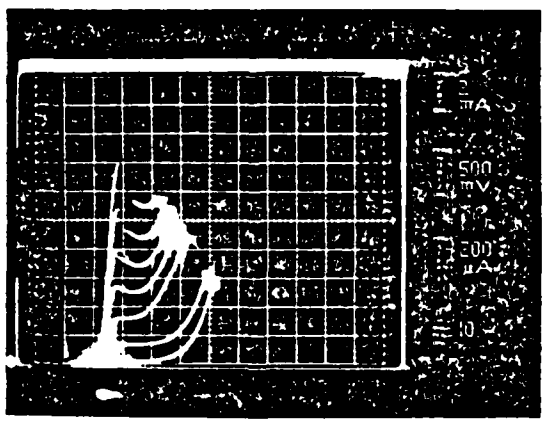


Fig. 2.14 (a) Common base, and (b,c) common emitter curves for a Q3 transistor on wafer 114/1.

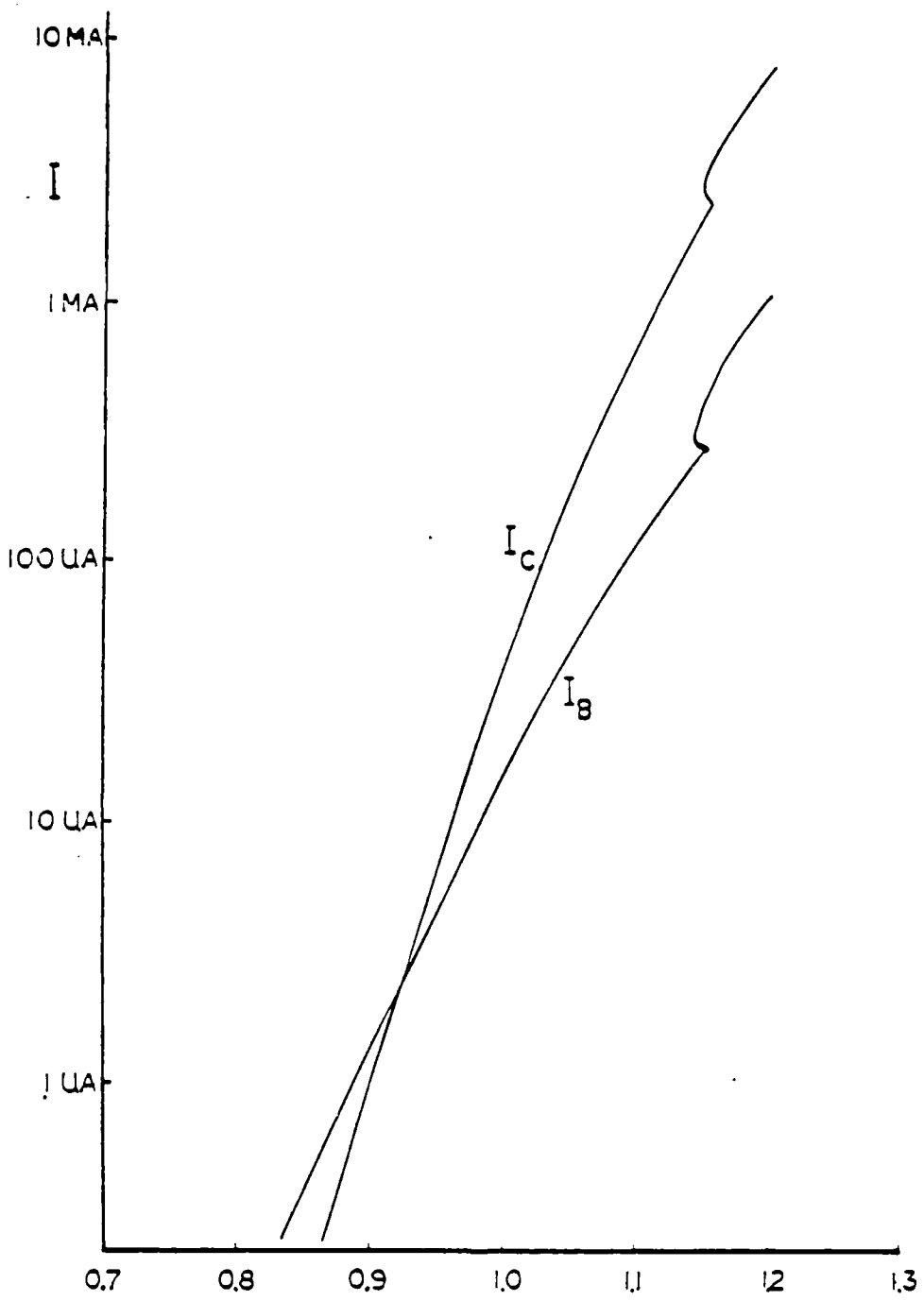


Fig. 2.15 Collector and base current versus emitter-base voltage for a Q3 transistor on wafer 114/1.

oscillation was found at 50MHz. This frequency is probably a resonance of the probe station. Oscillation begins at a current density of $10A/cm^2$. The oscillation is found even with the collector and base shorted together, forming a two-terminal device. This rules out the possiblity of simply having sufficient feedback to oscillate. It is important to note that no such oscillations were seen on the test diodes of wafer 114/2. We therefore rule out the emitter-base junction as the cause.

Examination of the I-V curves of the collector-base junction, shown in Fig. 2.16, shows an extremely low turn-on voltage. The ideality factor if 2 is probably coincidental, as the temperature dependence is very weak, corresponding to a bandgap of 0.56eV. It is far more probable that the current is carried by tunneling. The current scales with the area.

From all these considerations, it would appear likely that the cause for the behavior rests with the collector-base junction, and particularly with the high energy implant. We believe that the implant penetrated through the photoresist mask and modified the collector layer and probably also the base layer.

2.7. Summary and Conclusions

In the first section we reviewed the advantages of heterojunction transistors, and, in particular, of inverted heterojunction transistors. We then described an optimum structure for an emitter-base junction where an undoped graded layer is grown between the heavily doped emitter and base. This eliminates the heterojunction spike and the problems related to it, providing a minimum electron barrier and a maximum hole barrier. This structure had not been described in the literature when we began work on it and, as far as we know, ours is the only experimental work to date on this structure. We have also proposed a new structure for the same purpose in which the junction is not graded, but an undoped layer is grown on the narrow-gap side. This moves the peak of the spike below the level of the conduction band in the base. This structure is technologically more attractive because grading is not required. Finally, we have described the depletion-region recombination in a graded-gap structure, within the framework of the Sah-Noyce-Shockley model. We find that the resulting current has an ideality factor somewhat less than 2.

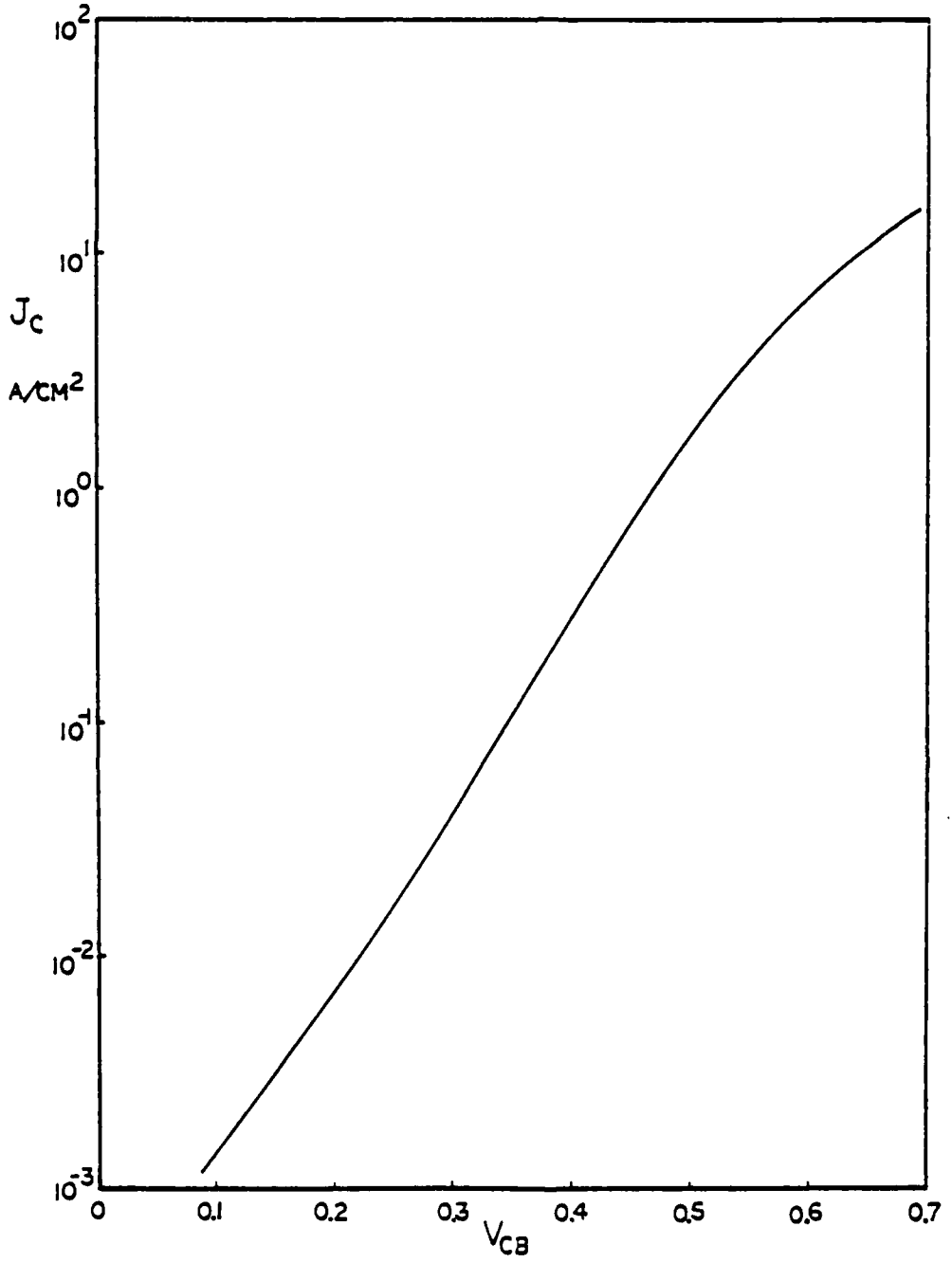


Fig. 2.16 Forward I-V characteristics of the collector-base junction of a Q3 transistor on wafer 114/1.

In the second section we described the experimental development of inverted (Al,Ga)As transistors by MBE. Experiments on emitter-base diode structures demonstrated that the proposed structures with undoped layers, both graded and abrupt, produced superior results. We also demonstrated a significant improvement in the quality of the heterojunction on top of the (Al,Ga)As layer when a "cleanup superlattice" was used. This is an important result for this type of device.

Ion implanted diodes were investigated in order to develop the technology required for blocking the injection in the external base region. It was found that furnace annealing provided better results than rapid thermal annealing, but optimum results were not achieved on these diodes.

Transistors were grown with a thicker emitter layer, made possible by use of a "cleanup superlattice." On these devices the external emitter-base junction was successfully converted to wide-gap and showed no sign of recombination current. The reduction in current, however, was not as great as predicted by the increase in energy gap. This was attributed to the back-injection of holes. Unfortunately, these devices did not show the expected performance. A maximum current gain of 10 was again observed. At high current levels the devices were found to oscillate at 50MHz. It was shown that this was caused by the high energy implant penetrating the photoresist mask.

If we have not succeeded in fabricating superlative devices, we have at least demonstrated the possibility of doing so. High internal gain and blocking of the unwanted injection have been achieved, although not simultaneously. A large fraction of the obstacles we faced were related to the maturity of the general level of technology within our laboratory, but there are several more fundamental questions that need to be addressed. The most pressing of these is to find an improved technique for blocking injection in the external region that will not damage the rest of the device. If this is to be done by implantation it will be necessary to find a more opaque masking technique. Improved annealing may also be necessary. Alternatively, some sort of diffusion might be used. The most promising form of this would be from a solid source on the surface, such as sputtered or deposited zinc oxide. A high degree of control and good lateral resolution and masking will be necessary.

Another area that needs attention is the collector-base junction breakdown. This will probably be intimately tied to the technology used for the injection blocking, and will probably involve some self-aligned processing.

Once the injection blocking is made highly effective it should be possible to empirically optimize the emitter-base junction with respect to growth parameters and structure.

Finally, it will be desirable to build devices with a graded composition in the base to provide a quasielectric field to assist the transport across the base.

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3. InGaP/GaAs HETEROSTRUCTURES BY MBE

3.1 The motivation for MBE of (Ga,In)P on GaAs

The overwhelming majority of all heterostructure work continues to be performed on the (Al,Ga)As/GaAs system, in which very good lattice match is automatically obtained over the entire composition range. The (Ga,In)P solid solution with a composition $Ga_{0.51}In_{0.49}P$ is also lattice-matched to GaAs, and this composition forms a potential alternate to (Al,Ga)As [1]. The original motivation for the investigation of the (Ga,In)P/GaAs heterostructure system was the desire to obtain a more optimal band lineup in the heterostructure bipolar transistors (HBTs). Ideally, the conduction band offset at an (abrupt) emitter-base junction in a HBT should be as small as possible, with a large valence band offset. The band lineups in the almost universally used (Al,Ga)As/GaAs system, as they had been determined experimentally during the late-70's, exhibited an large conduction band offset (typically, for 30% Al, 0.32eV) and a corresponding small valence band offset (typically 0.06eV). To obliterate the resulting undesirable conduction band spike barrier, the emitter-base junction was compositionally graded, which is technologically complex, and which appeared to introduce defects at the interface. These, in turn, were suspected to be at least partially responsible for the fact that HBTs have so far never lived up to their theoretical performance potential, even if the emitter-base junction was graded. It had been predicted theoretically [2] that the (Ga,In)P/GaAs heterojunction (HJ) would have a much more desirable band lineup, with a smaller conduction band offset (0.16eV) and a much larger valence band offset (0.29eV). Also, because (Ga,In)P does not contain aluminium, it would not be likely to exhibit the troublesome extremely high sensitivity of (Al,Ga)As to residual oxygen and carbon contamination, but would more likely behave like GaAs in this respect. During 1984, in work undertaken in this laboratory by M. Mondry, the first HBTs employing a (Ga,In)P emitter was constructed under a University of California MICRO project [3].

During the second half of 1984, the then widely accepted experimental data for the band lineups in the (Al,Ga)As/GaAs system suddenly came under suspicion, and by early-1985 there could no longer be any doubt that the conduction band offsets in the

(Al,Ga)As/GaAs system were significantly smaller (typically 0.25eV) [2] and hence much less unfavourable for HBTs than had been believed. This reduced somewhat the incentive for the development of an alternate (Ga,In)P technology, especially in the face of experience gained during 1983 and 1984 by M. Mondry and E. J. Caine in this laboratory, that such a technology was far more difficult than had been believed on the basis of their earlier very favourable experiences with straight GaP. Finally, the revision of the band lineups in the (Al,Ga)As/GaAs system [2] raised serious doubts about the validity of the theoretical predictions for the band lineups in the (Ga,In)P/GaAs system : these predictions had been based on Harrison's theory of band lineups [4], which until 1984 had been widely accepted as being remarkably reliable. It turned out that the revised band lineups in the (Al,Ga)As/GaAs system were in flagrant contradiction to that theory, thus destroying the credibility of that theory also for other hetero-systems.

This combination of circumstances called for an experimental determination of the band lineups in the (Ga,In)P/GaAs system, before continuing the development of the difficult technology for that system. This determination was undertaken and successfully completed in the present work.

3.2. MBE growth details and epi-layer characterization

3.2.1 Sample preparation and growth procedure

(Ga,In)P layers were grown by Molecular Beam Epitaxy (MBE) in a Varian-360 MBE machine, on (100)-oriented GaAs substrates. Silicon (Si) and Beryllium (Be) were used as n and p-type dopants respectively.

The GaAs substrates were cleaned in organic solvents, and etched in $NH_4OH : H_2O_2 : H_2O = 2 : 1 : 20$ for 2 min at room temperature. This was followed by a 10 min rinse in de-ionized (DI) water to form a native oxide. The oxide was desorbed in the MBE machine under an arsenic background, at a substrate temperature of 600°C for 7 min, until a streaky 2 x 4 surface reconstruction was observed via Reflection High Energy Electron Diffraction (RHEED). GaAs epi-layers were grown at 605°C, at a growth rate of 0.35 μm/hr. The arsenic to gallium *atomic* flux ratio ($2As_2$: Ga) was approximately 3 : 1. After the growth of the GaAs epi-layer the arsenic source (a GaAs decomposition source in the present case)

was cooled and the phosphorus source was heated up. This changeover took approximately 45 min. The P_2 source consisted of GaP in a furnace equipped with a special baffle [5] to condense out any gallium in the P_2 beam. The differential P_2 pressure at the substrate position was measured by a nude ionization gauge to be about 8 x 10^{-6} torr when the P_2 source furnace temperature was about 1130°C. It was found that (Ga,In)P layers with poor morphology and poor optical properties were obtained for P_2 pressures below this value. The (Ga,In)P epi-layer was nucleated at a substrate temperature of 505°C, at a growth rate of approximately 0.7 μm/hr.

3.2.2 Growth temperature limitation

In their study of the growth of (Ga,In)As and (Ga,In)P by MBE, Foxon and Joyce [6] concluded that the principal limitation to the growth of III-III-V alloy films by MBE is simply the thermal stability of the less stable of the two III-V compounds of which the alloy may be considered to be composed. They established that for the growth of III-III-V ternary alloys, two surface processes can occur which seriously impair compositional uniformity and control. These are, respectively, preferential desorption of the group V element, and, at some higher temperature, preferential desorption of one of the group III elements.

In the case of (Ga,In)P, InP is thermally much less stable than GaP. The congruent evaporation temperature of InP is about 365°C [7], while that of GaP is 672°C [8]. We have selected a growth temperature in the range 500 to 510°C for the growth of the (Ga,In)P epi-layers. At higher temperatures (550 to 580°C), P_2 desorbs to leave a surface with an enriched gallium and indium atom population. In principle, this loss by desorption could be balanced by increasing the incident P_2 flux, but in practice, as the temperature is increased, the required flux becomes impracticably high.

3.2.3 Characterization of the (Ga,In)P epi-layers

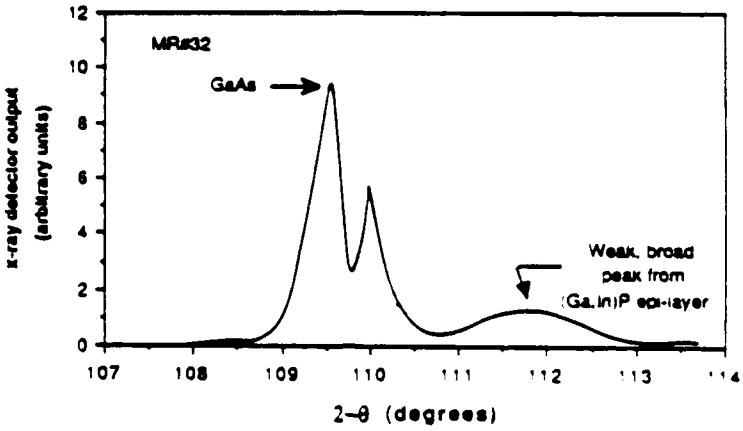
(Ga,In)P epi-layers were characterized via surface morphology, RHEED, X-ray 2θ-diffractometry, and photoluminescence. The results of these analytical techniques depend on the growth conditions i.e. the ratio of the group III fluxes (degree of mismatch), the

ratio of the *atomic* phosphorus flux to the total group III flux, and the growth temperature. Except where mentioned, the growth temperature was 505°C.

It was found that for phosphorus pressures less than about 5 x 10^{-6} torr, the layers were rough as seen with an optical microscope under differential interference contrast. These layers had a characteristic surface haze that appeared milky to the naked eye. The RHEED pattern was observed to be spotted during the layer growth. X-ray 2θ-diffractometry was done on these samples, and a typical 2θ scan is shown in Fig. 3.1 (a). One can clearly see two distinct $K\alpha_1$ and $K\alpha_2$ peaks from the GaAs substrate. However, there is just one broad and weak peak from the (Ga,In)P epi-layer. Low temperature (2 K) pumped liquid He photoluminescence (PL) measurements done on these samples showed a very weak peak at approximately 7150 Å or 1.738 eV. The full width at half maximum (FWHM) for this emission was approximately 187 meV. At first, it might seem that the poor morphology, spotted RHEED, weak X-ray and PL peaks might have been due to the large lattice mismatch between the epilayer and the substrate. However, this reasoning is probably invalid, in view of the following.

When the P_2 pressure was raised to about 8-9 x 10^{-6} torr in another run, it was found that the surface haze disappeared. The RHEED pattern was streaked and the surface reconstruction was 2 x 4 throughout the growth of the epi-layer. X-ray measurements now indicated two sharp $K\alpha_1$ and $K\alpha_2$ peaks from the epi-layer, at about the same angle where the single broad and weak peak was observed as described above (Fig. 3.1 (b)). A strong PL peak (10^3 times stronger than the PL peak mentioned above) was observed at 6400 Å or 1.941 eV. In other words, for approximately the same degree of mismatch, the higher P_2 pressure gave epi-layers with greatly improved optical qualities.

Different surface morphologies could now be seen for epi-layers grown with high P_2 fluxes. When the epi-layer is indium-rich (with a relative mismatch of +10 x 10^{-3}, x = 0.36) the epi-layer is under compression and there appears a strong cross hatching. This is believed to be associated with arrays of misfit dislocations. When the epi-layer is closely lattice matched to the surface (mismatch less than 10^{-4}, x = 0.51) the morphology of the grown layer is nearly indistinguishable from that of the substrate. There appear to be a few defects scattered about whose density is roughly 10^4 cm^{-2}. This suggests that these defects



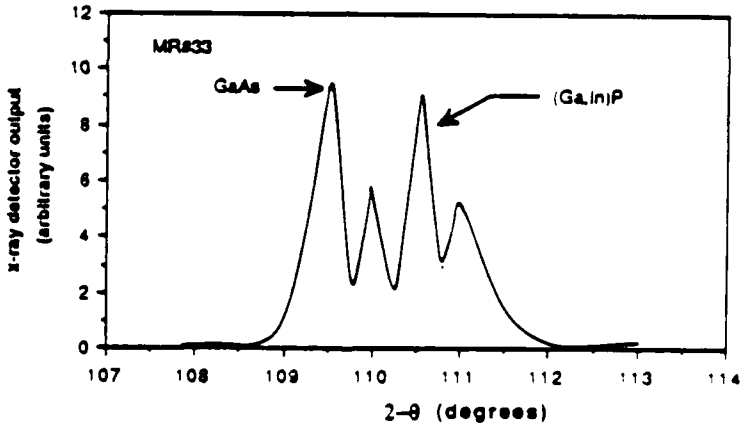


Fig. 3.1 X-ray 2θ- diffractometry scans on (Ga,In)P epi-layers grown with different P_2 pressures: (a) less than 5×10^{-6} torr; (b) greater than 8×10^{-6} torr.

may be related to or generated by dislocations from the substrate, because the dislocation count in the LEC grown GaAs crystals used for the substrate is typically 10^4 cm^{-2}. For a gallium-rich epi-layer (with a relative mismatch of -11 x 10^{-4}, x = 0.69) the epi-layer is under tension and the surface appears rough and fragmented along one of the ⟨110⟩ directions. Similar behavior of surface morphology in relation to lattice mismatch has been observed by Miller and McFee [9] in their work on the MBE growth of $Ga_xIn_{1-x}As$ on InP.

The best sample grown had a relative mismatch less than 10^{-4}. The X-ray 2θ-diffractometry scan for this sample is shown in Fig. 3.2. It can be seen that the $K\alpha_1$ and $K\alpha_2$ peaks from the epi-layer and substrate have merged into one another.

3.3. Determination of valence and conduction band discontinuities at the (Ga,In)P/GaAs heterojunction by C-V profiling

The method employed was capacitance-voltage (C-V) profiling through isotype heterojunctions, a technique introduced for determining band offsets at hetero-interfaces by Kroemer et al. [10], and recently employed with considerable success by several authors [11-14]. Both p-p and n-n heterojunctions were profiled, in order to obtain separate and *independent* values for both the valence band edge discontinuity (ΔE_V) and the conduction band discontinuity (ΔE_C), to permit the powerful self-consistency check of whether or not the values of the two discontinuities add up to the known energy gap difference (ΔE_g) between the two materials, as in the work of Watanabe et al. [14].

An additional check was performed, by comparing the actual experimental profiles with computer reconstructions of what the C-V profiles *should have been* for the particular band offset data found, *if* the heterojunctions satisfied the simple theoretical model of a perfectly abrupt junction.

3.3.1 Sample structures

As described in section 3.2.1 epitaxial layers of (Ga,In)P and GaAs were grown by molecular beam epitaxy in a Varian-360 MBE machine, on (100)-oriented, Si-doped n^+-GaAs substrates. Both n-n and p-p isotype structures were grown, for separate ΔE_C and ΔE_V measurements. X-ray diffractometer data were taken on all layers grown, and layers

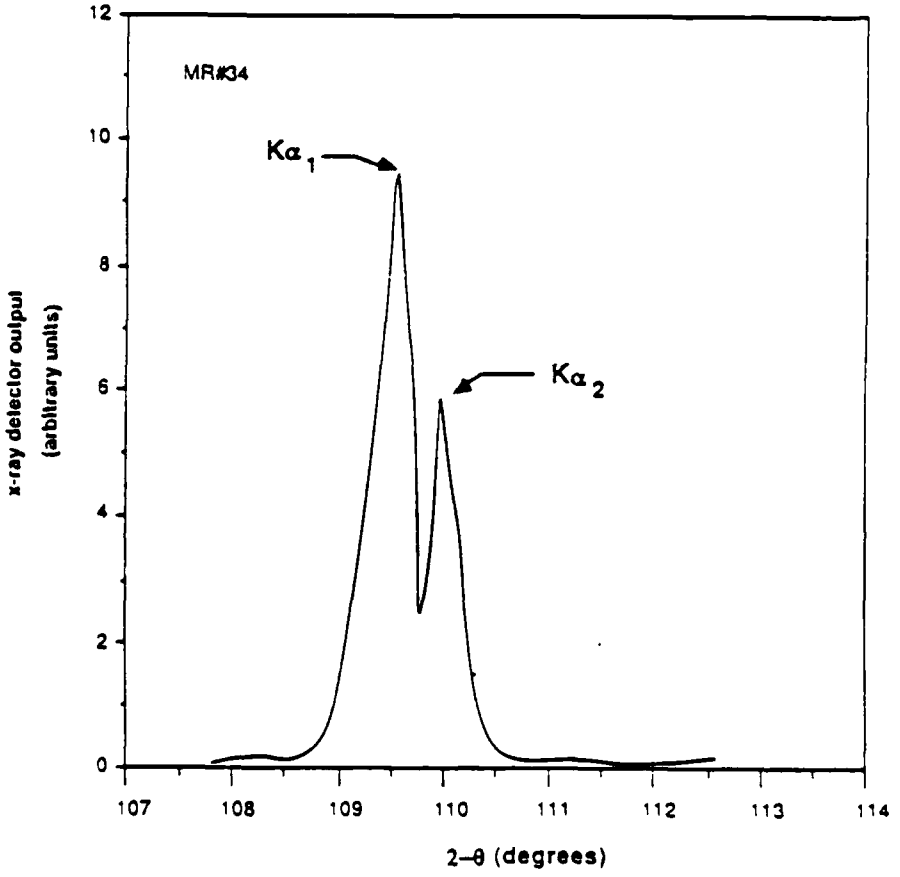


Fig. 3.2 X-ray 2θ- diffractometry scan for a very closely lattice-matched epi-layer (relative mismatch less than 10^{-4}). The $K\alpha_1$ and $K\alpha_2$ peaks from the epi-layer and substrate can be seen to be merged into one another.

with unsatisfactory lattice match were discarded. On our best n-n sample, diffractometry indicated that the (Ga,In)P epi-layer was slightly gallium-rich with a relative lattice mismatch of approximately 10^{-3}, while on our best p-p sample a much smaller relative lattice mismatch of less than 10^{-4} was achieved. These were the two samples on which detailed C-V profiling studies were performed, reported here. The overall structures, with the thicknesses and doping levels of the layers, were as shown in Fig. 3.3. With the n-n structures, the profiling was conducted from a reverse-biased aluminum Schottky barrier deposited on the n-(Ga,In)P surface (Fig. 3.3a). Because Schottky barriers on p-(Ga,In)P were too leaky to permit C-V profiling, the profiling of the p-p heterojunctions (HJs) was carried out by continuing to use an n^+- substrate, and profiling upward from the reverse-biased n^+- p junction between the substrate and the p-GaAs epi-layer (Fig. 3.3b). The schematic energy band diagrams of the HJ portion of the two structures are shown in Fig. 3.4, both oriented such that the profiling direction is from the left to the right.

3.3.2 Preparation of samples for C-V profiling

On the n-n samples, aluminum Schottky barriers were fabricated by deposition and lift-off. The diode area was 4.8×10^{-4} cm^2. On the p-p samples, Au-Zn dots were deposited by evaporation and lift-off, and alloyed at 450°C for 30 sec on a graphite strip heater, to form an ohmic contact to the p-(Ga,In)P. Diode mesas were then formed by etching the (Ga,In)P with HCl : H_3PO_4 = 1 : 1. We found that this etchant produced less undercutting than the undiluted HCl etch commonly used for etching (Ga,In)P. Following the (Ga,In)P etch, the p-GaAs was etched with $H_3PO_4 : H_2O_2 : H_20 = 5 : 1 : 14$, to a depth sufficient to reach into the n^+-substrate. The final p-p diode mesa area was measured to be 4.6×10^{-4} cm^2. The return contact for both n-n and p-p structures was formed by indium alloyed to the n^+-substrate.

3.3.3 C-V Profiling : results and discussion

ΔE_V measurements

Because we found the p-p results more trustworthy, they are discussed first. As stated earlier, the C-V profile through the p-(Ga,In)P/p-GaAs HJ was obtained by reverse

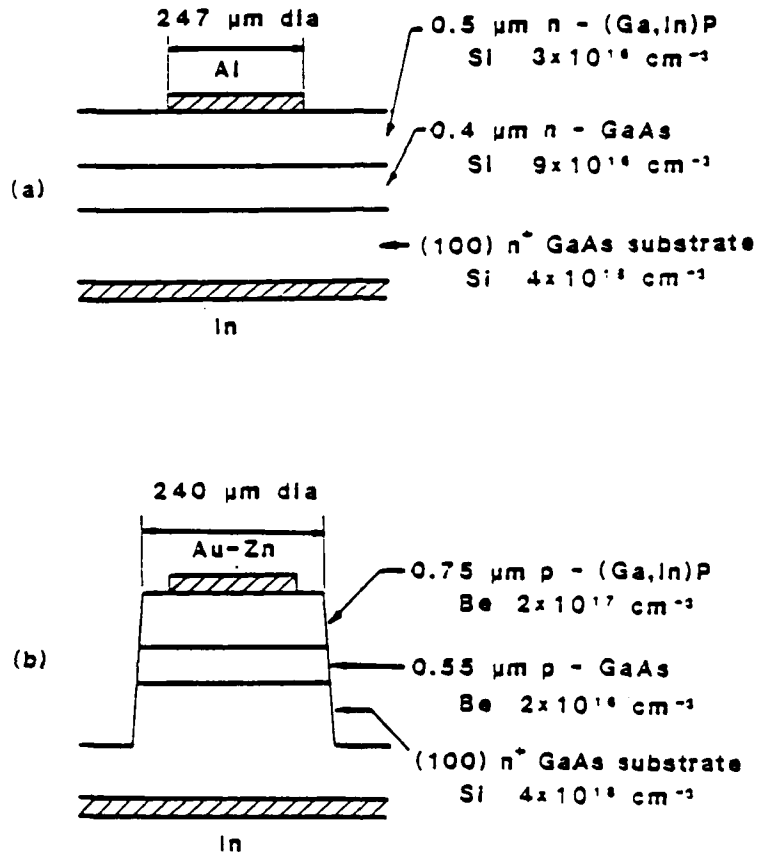


Fig. 3.3 Structure of samples for C-V Profiling: (a) Sample for determination of conduction band offset by profiling through an n-n junction from a surface Schottky barrier; (b) Sample for determination of valence band offset by profiling through a p-p junction from a buried n^+-p junction.

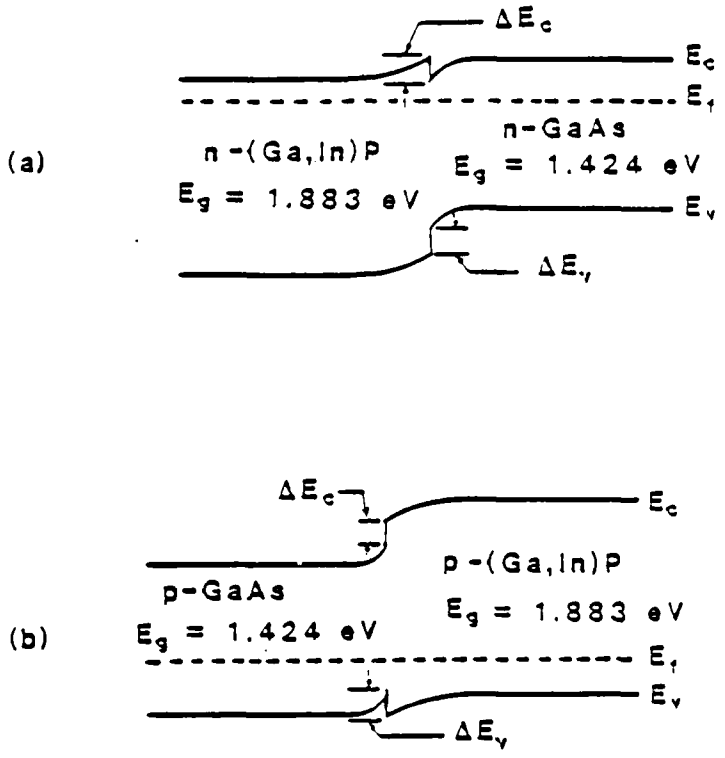


Fig. 3.4 Expected band diagrams (a) for the n-n heterojunction; (b) for the p-p heterojunction. Both are oriented such that the profiling direction is from the left to the right.

biasing the n^+- p junction between the substrate and the p-GaAs epi-layer, shown in Fig. 3.5b. A HP4280A C-V meter was used for the measurement. The measurement frequency was 1MHz, and the magnitude of the applied differential voltage was 30 mV (rms). The *apparent* majority carrier concentration profile p*(x) was derived from the C-V profile according to the standard relation

$$p^*(x) = \frac{2}{q\varepsilon}\left[\frac{d}{dV}\frac{1}{C^2}\right]^{-1} \qquad (3.3.1)$$

where

$$x = \varepsilon / C \qquad (3.3.2)$$

is the width of the depletion layer, essentially the distance of the depletion layer edge from the p-n junction. The various symbols in (3.3.1) and (3.3.2) have the following meaning:

p*(x) : apparent majority carrier (hole) concentration at position x;

V : reverse bias voltage;

C : capacitance per unit area;

ε : dielectric permittivity of the semiconductor [15].

An experimental apparent carrier concentration profile is shown as a solid line in Fig. 3.5. Hole accumulation is seen in the GaAs, and a depletion region in the (Ga,In)P, as expected from the band diagram of Fig. 3.4b. The doping in the n^+-substrate, 4×10^{18} cm^{-3}, was sufficiently large that the correction to the profile due to a small amount of depletion into the substrate could be neglected. Also shown in Fig. 3.5, as a broken curve, is a "best fit" computer-generated theoretical p*(x) profile, which will be discussed later.

The value of ΔE_V is obtained from the electrostatic dipole moment that is associated with the charge imbalance between a presumably known doping distribution P(x) and the experimental p*(x) curve, using the relation given by Kroemer et al. [10], adapted to the p-p case :

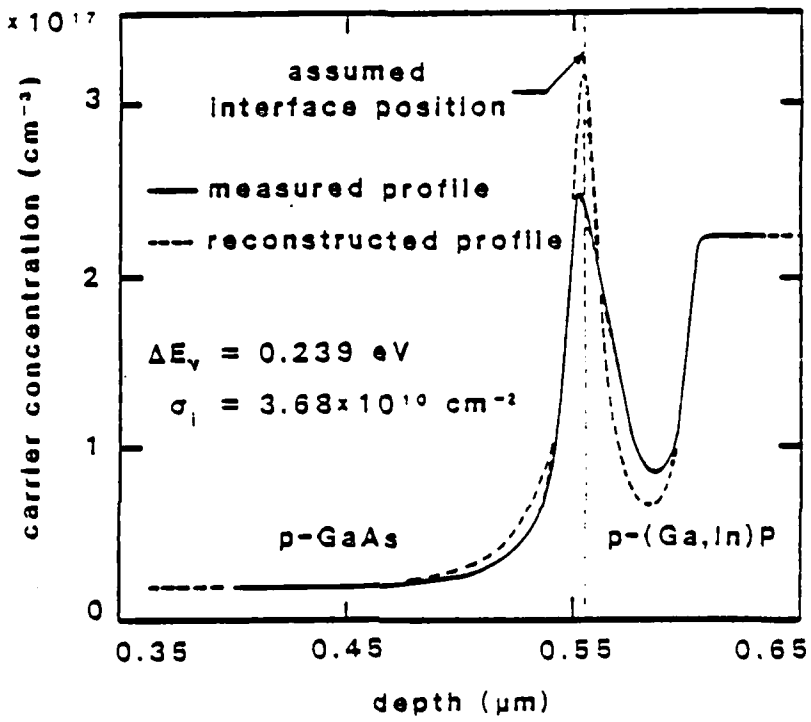


Fig. 3.5 Experimental and reconstructed apparent carrier concentration profiles for the p-p structure.

$$\Delta E_v = \frac{q^2}{\varepsilon} \int_0^{\infty} [P(x) - p^*(x)] \cdot (x - x_1)\, dx - kT \cdot \ln\left[\frac{P_2 N_{V1}}{P_1 N_{V2}}\right] \qquad (3.3.3)$$

Here the newly-introduced symbols have the following meaning :

ΔE_V: valence band edge discontinuity, counted positive if the step is upward when going from the (Ga,In)P towards the (GaAs), as assumed in Fig. 3.4b;

$P(x)$: ionized acceptor distribution, assumed to be known and to level out far away from the HJ;

$P_{1,2}$: asymptotic values of the doping levels in the GaAs (#1) and the (Ga,In)P (#2)

x_i : distance of the HJ interface from the n+- p junction;

$N_{V1,2}$: valence band density of states in the two regions.

An accurate determination of P_1 and P_2 is necessary if the band discontinuity is to be obtained with confidence. It can be seen from the $p^*(x)$ curve that the hole concentrations on both sides of the HJ leveled out very well; thus P_1 and P_2 could be accurately established.

To evaluate (3.3.3), we assumed a model of uniform doping on both sides of the interface plane $x = x_i$, with an abrupt step in the doping at $x = x_i$, as well as the existence of a localized interface defect charge σ_i at $x = x_i$. For a given value of x_i the value of σ_i is obtained from the requirement of overall charge neutrality [10] :

$$\sigma_i = \int_0^{\infty} [p^*(x) - P(x)]\, dx \qquad (3.3.4)$$

In such a model an accurate knowledge of the interface position x_i is essential. Although a *nominal* value for the thickness of the GaAs layer was known from the growth rate, the accuracy of this value was not sufficient for use in determining ΔE_V reliably, and the value of x_i had to be determined, as usually, from the profile itself. To this end a *series* of values of ΔE_V and of the interface charge density σ_i were calculated from (3.3.3)

and (3.3.4), for a series of *assumed* values of the interface position x_i around the neutral value. We then obtained a computer reconstruction of what the p*(x) profile *should have been* for an abrupt junction with given values of band offset and interface charge, using a computer program that basically solves Poisson's Equation for incremental voltage steps applied to the HJ [16]. Such a computer reconstruction had been found useful in our earlier work [10], and more recently it was used with excellent success by Watanabe et al. [14].

Specifically, we calculated values of ΔE_V and σ_i from the experimental p*(x) profile for a range of assumed values of x_i, and used them to reconstruct numerically the apparent carrier concentration profiles associated with the different sets of values. These were then compared with the experimental profile for each of the assumed x_i values, as in the work of Watanabe et al. [14]. The broken curve in Fig. 3.5 shows the best overall fit that could be obtained for our p-p junction, for x_i = 0.555 μm, yielding ΔE_V = 0.239 eV and σ_i = +3.68 x10^{10}, cm^{-2}, near but not exactly at the band offset minimum. Note that the change in band offset from the value at the minimum is only 1meV. Although we were unable to obtain as close a fit as in the better samples of the work of Watanabe et al. [14], or of our own earlier work [10] on (Al,Ga)As/GaAs, the agreement between the experimental and reconstructed profiles is quite good. The remaining discrepancies must be viewed either as due to experimental errors, or as indications that our model of a perfectly abrupt interface is not fully applicable, but it is difficult to say more.

Expressed as a fraction of the known total energy gap difference, $\Delta E_g \approx 0.45$eV [17], our ΔE_V-value corresponds to 0.52 ΔE_g. This value is about 50 meV smaller than the originally predicted $\Delta E_V \approx 0.29\text{eV} \approx 0.63\ \Delta E_g$ for the lattice-matched $Ga_{0.51}In_{0.49}P$/GaAs interface, obtained by simple linear interpolation [18] between the theoretical valence band offsets for GaP/GaAs and InP/GaAs that are predicted by the Harrison theory [19]. Although not negligible, this discrepancy is actually smaller than the discrepancy between experiment and prediction from the Harrison theory for most hetero-systems.

3.3.4 ΔE_C measurements

The structure shown in Fig. 3.3(a) was used to measure ΔE_C. The aluminum Schottky barrier was reverse-biased to obtain a C-V profile through the HJ. The analysis of the data was analogous to that for the p-p structure. Fig. 3.6 shows the experimental

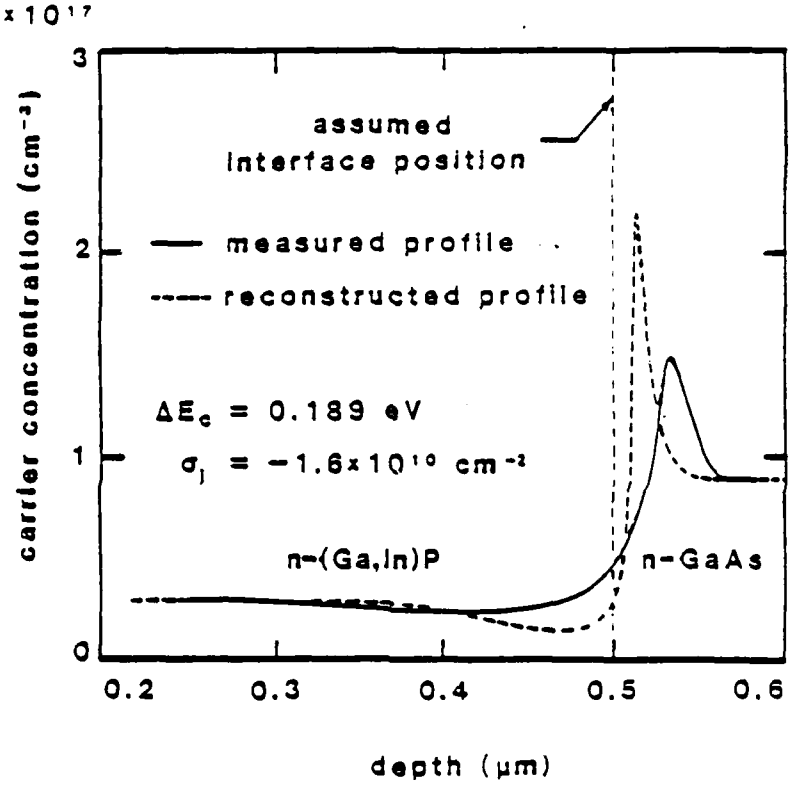


Fig. 3.6 Experimental and reconstructed apparent carrier concentration profiles for the n-n structure.

carrier concentration profile, in which electron accumulation and depletion can be seen in the GaAs and (Ga,In)P, again as expected from the predicted energy band diagram shown in Fig. 3.4a.

We were not able to obtain a good a fit between experimental and reconstructed carrier concentration profiles. The reconstructed profile shown in Fig. 3.6 represents the "least bad" fit, corresponding to the triplet $x_i = 0.500$ μm, $\Delta E_c = 0.189$ eV, $\sigma_i = -1.6 \times 10^{10}$ cm^{-2}. Again this profile is one with a small interface charge, and again the value of the band offset is not very sensitive to the choice of x_i. But the peak-to-valley concentration ratio of the experimental profile is lower, and the peak and valley are separated farther in space than in the reconstructed profile. This combination indicates that the ionized impurity profile and/or the energy gap of the actual junction must be graded at the transition, in contrast to the mathematical model used in the reconstruction, which assumed an abrupt transition at the interface for both. MBE-grown junctions tend to be compositionally quite abrupt [20], and it would in fact be difficult to explain an unintentional compositional grading wide enough to explain the discrepancy between the two curves in Fig. 3.6, but impurity diffusion or carryover could easily have taken place. If one inspects the n-n equivalent of (3.3.3) for our case of a heavier doping on the GaAs side, one finds readily that the presence of a doping gradient at the interface causes an *increase* in the value of ΔE_c relative to the abrupt-model value. In fact, our raw band offset data add up only to $\Delta E_v + \Delta E_c = 0.428$ eV, a value 31 meV smaller than the *known* energy gap difference $\Delta E_g \approx 0.459$ eV, a discrepancy of about 7%, giving further credence to the assumption of a graded impurity profile.

To estimate the effect of grading on the calculated band offset value, at least to a first order, the doping gradient may be approximated by a straight line, with a half width equal to the distance between the accumulation and depletion extrema in the experimental profile, as shown in Fig. 3.7. The contribution of the grading to the electrostatic dipole moment would then be simply that of the two shaded triangles, about 24 meV, within 7 meV of the band offset sum discrepancy of 31 meV. A gradient only 14% wider would have yielded the full discrepancy. Although the estimate is crude, it is clear that the correction is quite close to the discrepancy, lending strong support to the hypothesis that most of the discrepancy is due to grading of the ionized impurity concentration. A more accurate check

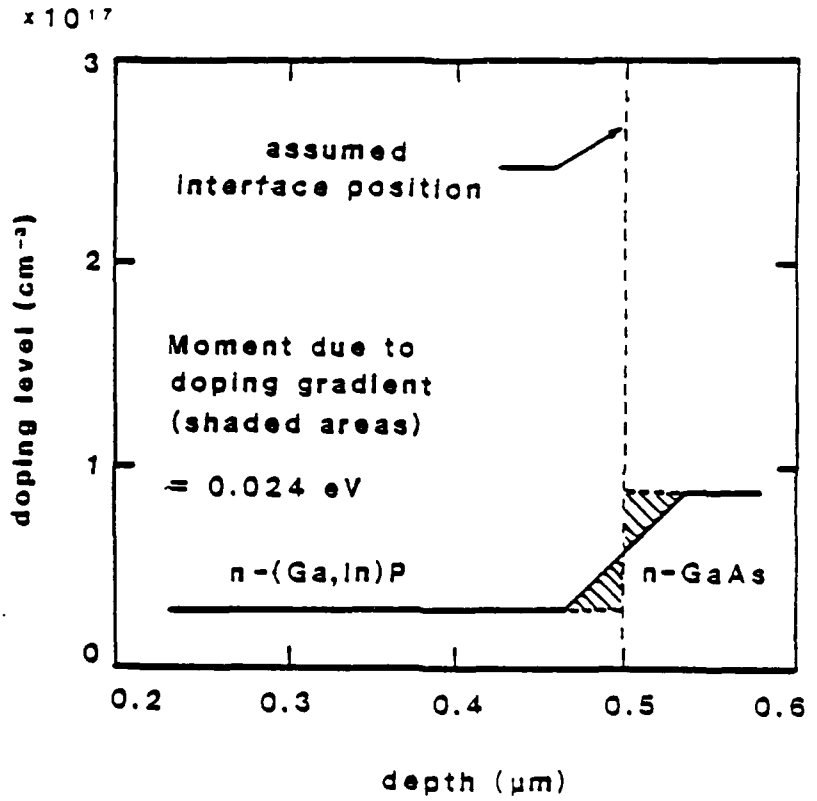


Fig. 3.7 Simple model for the doping gradient postulated to be present in the n-n heterojunction.

would have been a computer reconstruction using a graded profile with a more realistic graded profile, but we do not currently have a suitable computer program for such more advanced reconstructions available.

Presumably, some grading might also be present at the p-p junctions, but the amount is clearly much smaller, and any correction to the valence band offset would be quadratically smaller. Within the accuracy of our data we may therefore allocate the entire discrepancy to the conduction band offset, yielding a corrected conduction band offset of $\Delta E_C \approx 0.22$ eV $\approx 0.48\ \Delta E_g$. The value of ΔE_C predicted from the Harrison model was 0.160 eV $\approx 0.35\ \Delta E_g$.

The origin of the postulated impurity gradient is not clear, but we suspect that it might be due to strain-induced diffusion: Studies of masked diffusion in GaAs [21] have shown the presence of large lateral diffusion of the diffusant in the presence of strain at the mask/GaAs interface. In those studies the masks were deposited films of silica, phosphosilicate glass, or silicon nitride, and the strain at the mask/GaAs interface was caused due to their different thermal expansion characteristics. In our n-n sample, significant outdiffusion of Si could have taken place at the GaAs/(Ga,In)P interface, due to strain caused by the non-negligible residual lattice mismatch in that sample. In contrast, it should be recalled that the p-p isotype interface was relatively strain-free.

A comment is in order concerning the possibility that in addition to the impurity gradient there might be a gradient in the energy gap present. The n-n equivalent of (3.3.3) was originally derived for the case that the energy gap changes abruptly. It was subsequently shown [22] that the relation remains valid if the energy gap is graded, so long as the correct ionized impurity distribution is known and is used in the evaluation of (3.3.3). In this case the band offset derived from (3.3.3) is always that offset that would have been present *if* the junction had been abrupt. The energy gap variation does not enter the problem of offset determination; only a knowledge of the ionized impurity concentration P(x) -- or N(x) -- as function of position is required. However, in the presence of energy gap grading, the reconstruction of the apparent carrier concentration profile will fail, even if performed with correct values of the offset and the ionized impurity profile. For example, in the (unlikely) limit of a gradient in the energy gap alone, unaccompanied by a doping gradient, the experimental apparent electron concentration profile would be spread out, and

hence would lead to a failure of the reconstruction of this profile using an abrupt model. But in the evaluation of the conduction band offset from the n-n analog of (3.3.3), the effects of profile lowering and profile spreading would cancel out exactly [22], yielding the band offset value of the ungraded junction.

3.3.5 Comments on possible sources of errors

It is difficult to place an exact error estimate on our band offset values. The largest single source of uncertainty is the quality of our samples. Although C-V profiling is potentially a powerful and accurate method, its success depends far more on the quality of the samples than the published literature on the subject suggests. While we would have preferred to have samples of a quality approaching that of the (Al,Ga)As/GaAs HJ samples reported in the literature, that option was not available, given the state of the technology for the MBE growth of reasonably abrupt, well lattice-matched (Ga,In)P/GaAs HJs. In fact, the measurements reported here were themselves part of the early phases of the development of such a technology. Our p-p sample is clearly the better of the two samples, even if one ignores the evidence provided by the computer reconstructions of the two profiles: the sample has less lattice mismatch, and the C-V profile has a much more pronounced peak-and-valley structure, suggesting much less trouble from grading and from interface charge effects. However, without computer reconstruction it would be difficult to be more specific and to give an error estimate. The reconstruction fit, although far from perfect, is much better than for the n-n sample, suggesting that any errors due to impurity grading effects are much smaller than our earlier estimate of 20 to 30 meV for the grading correction in the n-n case, certainly below ±10 meV.

The principal potential source of any larger error could be deep levels at or near the interface, including, but not restricted to deep levels associated with misfit dislocations. By deep levels we mean here levels whose ionization changes with changing bias. Their effect on the apparent carrier concentration profile is at this time not understood, and conceivably they might introduce changes into the interpretation of these profiles that would lead to changes in the band offsets larger than our otherwise conservative error estimate for the p-p junctions. An investigation of such effects was beyond the scope of our work, and in the absence of any other evidence of such changes we believe that ignoring them is justified, at least for the p-p junctions.

Considering that we are quoting band lineups on the millivolt level, less than 2-3% of the overall energy gap difference, one natural area of concern is the extent to which the capacitance measurements themselves are sufficiently accurate. Practical experience with the accuracy of C-V profiling in the determination of doping profiles might suggest that such accuracies might be illusory. Surprisingly, however, many measurement errors that would lead to incorrect doping profiles cancel out in band offset determinations. Any error in the capacitance measurements *by a constant factor*, for example by an error in the diode area, cancels out of the band offsets: Although such an error would yield an incorrect apparent carrier concentration, it also yields an incorrect position allocated to this carrier concentration, and the two errors cancel *exactly* when the band offset is calculated [23]! Furthermore, even certain kinds of non-constant errors cancel out: It has been shown [15,16] that the permittivities of both semiconductors cancel out of the band offset, even if the two permittivities are different. Hence any measurement error that is mathematically equivalent to an error in the two permittivities cancels out.

3.3.6 Consequences of the (Ga,In)P/GaAs band lineup

As expected, the band lineup between (Ga,In)P and GaAs is of the straddling type. In summary it can be said that reasonable agreement between the experimental and reconstructed profiles was obtained for the p-p isotype structure, and the valence band discontinuity was obtained to be 0.24 eV, or $0.52\Delta E_g$. Comparison of the experimental and reconstructed profiles for the n-n isotype structure indicated the presence of significant grading at the interface. A first- order correction of the raw data to the measured ΔE_C was estimated, yielding a corrected value of ΔE_C of 0.21 eV, or 0.46 ΔE_g. These values of ΔE_V and ΔE_C , obtained from independent measurements, add up to 98% of ΔE_g, indicating good self-consistency, and suggesting an accuracy of the individual values themselves to probably better than ±10 meV. Because the grading correction for the n-n junction was based on a rather crude estimate, and because the two band offsets **must** add up to the known energy gap difference, we allocate the remaining 7 meV discrepancy to the conduction band offset, leading to a final value of ΔE_C of 0.22 eV, or 0.48 ΔE_g.

Our lineup data lead to interesting predictions for the band lineups for (Ga,In)P lattice-matched to $Al_xGa_{1-x}As$. In Fig. 3.8, taken from a recent review [24], we have

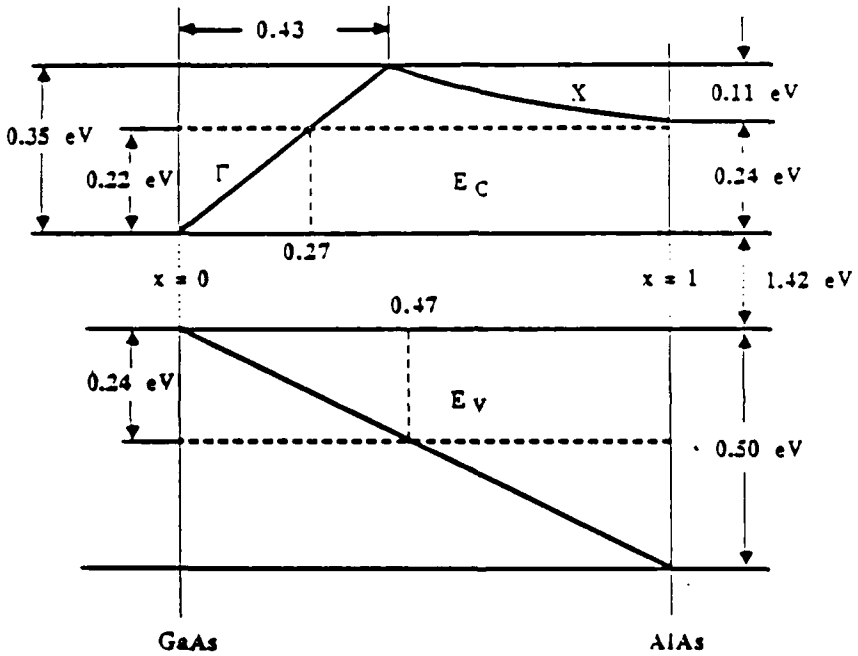


Fig. 3.8 Predicted relative band edge energies at (Ga,In)P/(Al,Ga)As.

superimposed our conduction and valence band edge energy values for (Ga,In)P on current "best estimate values" for the lineups *within* the $Al_xGa_{1-x}As$ alloy system [24]. It appears that the valence band of $Al_xGa_{1-x}As$ will drop below that of lattice-matched (Ga,In)P for $x > 0.47$. The conduction band offsets are more complicated, due to the Γ-to-X crossover in the $Al_xGa_{1-x}As$ band structure around $x = 0.43$. We estimate that the conduction band of $Al_xGa_{1-x}As$ will initially rise above that of (Ga,In)P for $x > 0.27$. For $x > 0.43$, the conduction band energy of $Al_xGa_{1-x}As$ drops again, and it should reach a value very close to the (Ga,In)P value as $x \rightarrow 1.0$. Thus there are likely to be three $Al_xGa_{1-x}As$ composition ranges with quite different behavior: (i) For $x < 0.27$, the band lineup should remain a straddling one, with $Al_xGa_{1-x}As$ retaining the lower total gap, and with a vanishing conduction band offset at the upper end of this range. (ii) For $0.27 < x < 0.47$, the system should be a staggered one, with (Ga,In)P having both band edges below those of $Al_xGa_{1-x}As$. The residual interface gap should slowly increase through this range, from about 1.78 eV for $x = 0.27$ to 1.95 eV for $x = 0.47$. This might be an interesting range for the study of staggered-lineup luminescence [25,26] in p-$Al_xGa_{1-x}As$/n-(Ga,In)P heterojunctions. (iii) For $x > 0.47$, the band lineup would become straddling again, but now with (Ga,In)P having the smaller energy gap.

It would appear that these band lineups might find applications in future electronic and optoelectronic device structures. With regard to the initial motivation for this work, the use of (Ga,In)P/GaAs HJs as emitters in HBTs, both our data and the recent re-assessments of the band lineups within the $Al_xGa_{1-x}As$ alloy system [24] diminish somewhat the attractiveness of that idea: The conduction band offsets in the (Ga,In)P/GaAs system are not quite as small as had been hoped, and those within the $Al_xGa_{1-x}As$ alloy system are not as large as had been feared. Together with the more difficult technology of (Ga,In)P relative to (Al,Ga)As, these changes conspire to reduce the incentive for (Ga,In)P as a material for HBTs, but probably not for other applications.

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4. NON-ALLOYED GRADED-GAP OHMIC CONTACTS

4.1 The (Ga,In)As n-type contact

One of the most troublesome areas of all compound semiconductor technology is that of the (so-called) ohmic contacts. The poorly understood and poorly reproducible Au/Ge/Ni and Au/Zn alloy contacts to n and p-type GaAs respectively, are rapidly emerging as severe limitations on the further progress of compound semiconductor devices.

In 1981 Woodall et al. [1] proposed and demonstrated a non-alloyed graded-gap scheme for obtaining ohmic contacts to n-type GaAs, by first growing a graded transition from GaAs to InAs and then making a non-alloyed metallic contact to the InAs. It is well known that at a metal-to-InAs interface the Fermi level is pinned inside the InAs conduction band [2], hence this interface by itself acts as an ideal negative-barrier ohmic contact. However, if the GaAs-to-InAs transition were not graded, it would act as a quasi-Schottky barrier with a barrier height close to the conduction band offset ΔE_c of the GaAs/InAs heterojunction, about 0.9eV [3], and the contact would be poor overall. Sufficient grading obliterates the heterojunction barrier, and leads to an excellent ohmic contact with properties that can be superior to the traditional, widely-used Au-Ge/Ni/Au alloyed system [4-6]. In fact, it is probably not necessary to grade all the way to InAs: Kajiyama et al. [7] have shown that a zero or negative surface barrier height exists for In:Ga ratios above 80:20. The band diagram for an abrupt GaAs/InAs interface and that for a graded GaAs/InAs interface is shown in Fig. 4.1.

In their work, Woodall et al. [1] graded over a rather large distance, about 2500 Å. For a negative surface barrier height, the series resistance of the graded transition region should be the dominant residual contribution to the contact resistance. This suggests using a graded region no longer than necessary for flattening out the bands. The necessary grading may be estimated as follows. If the transition region is graded over a width w, the graded offset is equivalent to an electric field $E_Q = \Delta E_c/qw$. This quasielectric field must be compensated by a true electric field, which must be supported by charges near the ends of the graded region. To insure a flat conduction band, the doping level must be sufficiently

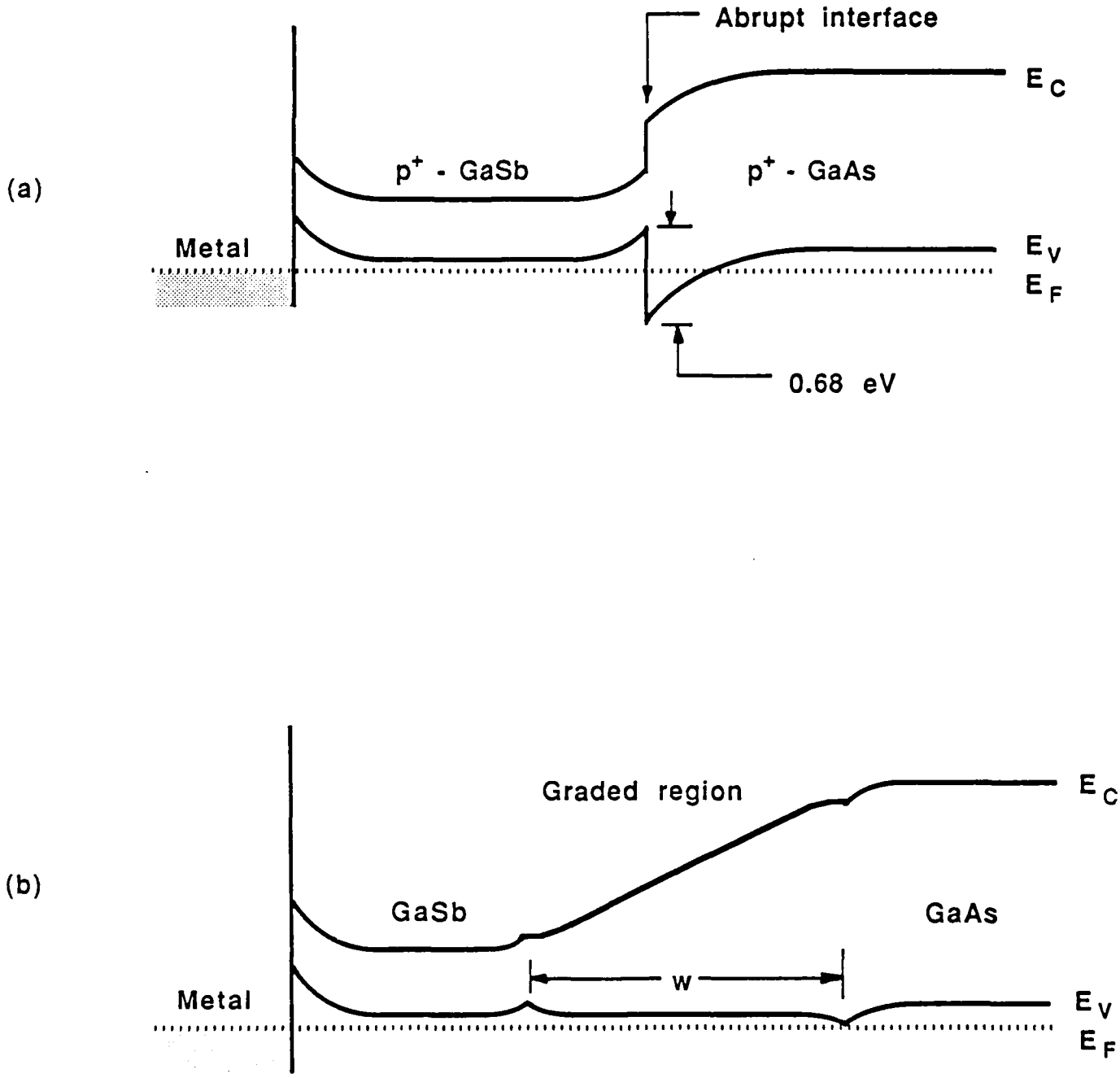


Fig. 4.1 Band diagrams for (a) an abrupt GaAs/GaSb interface, and (b) for a graded GaAs/GaSb interface.

high to make it possible to support this field with the donors contained in a region significantly thinner than the graded region itself. If N_D is the doping level and ε the permittivity of the semiconductor, this leads to the condition

$$q N_D w >> eE_Q = e\Delta E_c/qw, \text{ or } N_D w^2 >> e\Delta E_c/q^2 . \qquad (4.1.1)$$

Inserting numbers ($\varepsilon \approx 14\varepsilon_0$; $\Delta E_c \approx 0.9$eV) yields, on the right-hand side, 7×10^6 cm^{-1}. With doping levels of 1×10^{19}cm^{-3}, which have been demonstrated in GaAs [8], a more detailed analysis [9] shows that a safety margin of 10 is generous, corresponding to $w \geq 2.6\times10^{-6}$ cm as the required grading distance, about one-tenth the distance used by Woodall et al.

A doping level of 10^{19}cm^{-3} yields a resistivity below 6×10^{-3} Ωcm [8]. For a 260 Å thick transition layer this corresponds to a contact resistivity below 2×10^{-9} Ωcm^2. This value would be about a factor 35 below the lowest trustworthy value that has been reported for Au/Ge/Ni [6], and much lower than *typical* values for that system [5].

4.2 Ga(As,Sb) p-type contact

Analogously, at a metal-to-GaSb interface, the Fermi level is pinned inside the GaSb valence band, and hence the Ga(As,Sb) system would be suitable for p-type contacts. Band diagrams for the GaAs/GaSb system with and without grading are shown in Fig. 4.2. The theoretical analysis for the p-type graded-gap contact is similar to that for the n-type contact presented above in sec. 4.1. The theory predicts that contact resistivities below 2×10^{-8} Ωcm^2 should be possible for p-type contacts.

4.3 Graded-gap contact growth procedure

As a preliminary to transistors, n- and p- type graded-gap contacts grown by molecular beam epitaxy (MBE) on (100)-oriented semi-insulating GaAs substrates were investigated separately. For the n-type graded gap contact structures approximately 200nm of 1×10^{18} cm^{-3} (Si - doped) n$^+$- GaAs was grown at 600°C, with an arsenic-to-gallium atomic flux ratio of approximately 2 : 1. During the growth of the graded region the

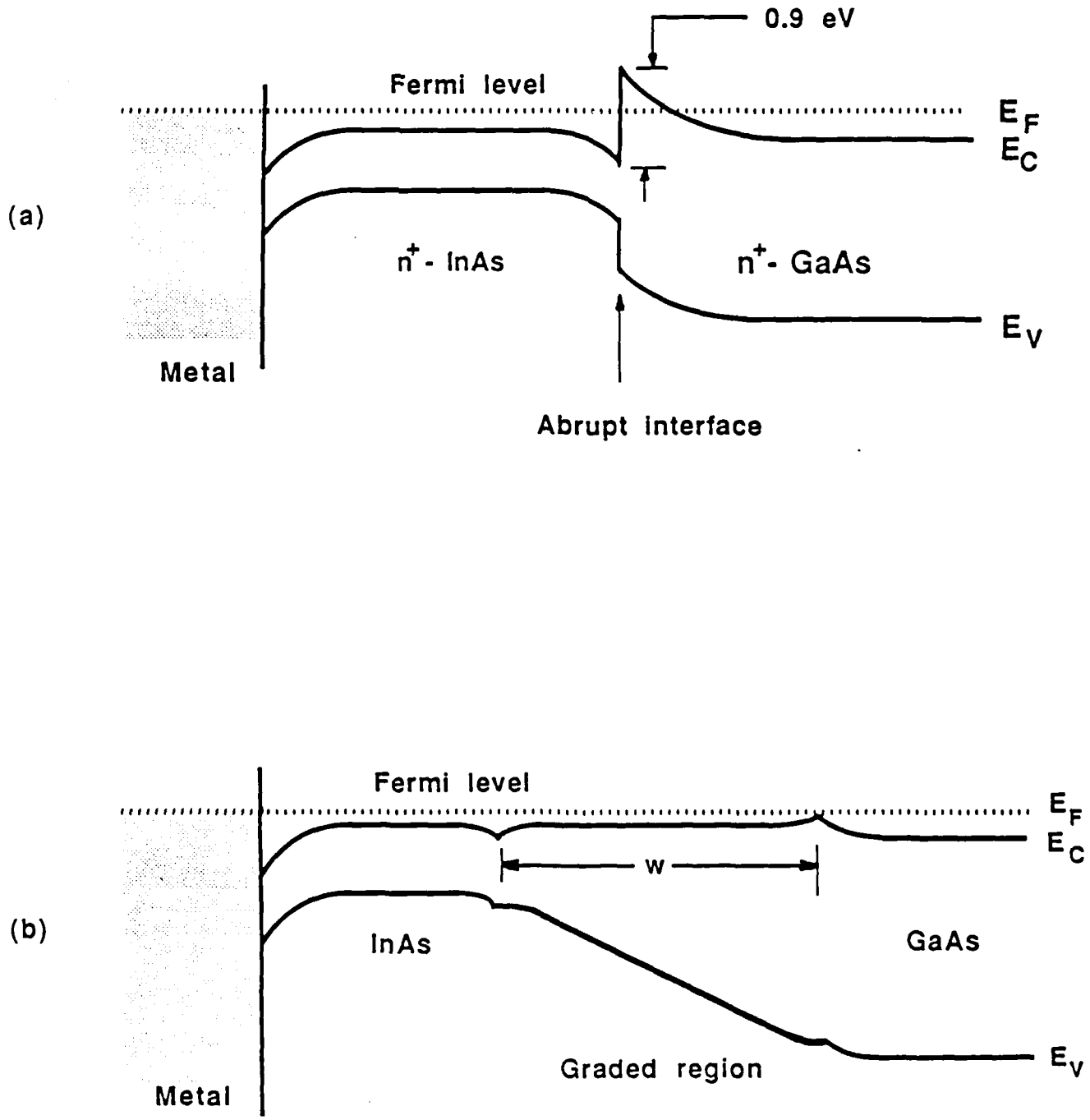


Fig.4.2 Band diagrams for (a) an abrupt GaAs/InAs interface, and (b) a graded GaAs/InAs interface.

substrate temperature was ramped down from 600°C to 500°C because the temperature of congruent sublimation for (Ga,In)As decreases with increasing indium fraction [10].

In order to keep the series path resistance of the graded region low, the doping in the graded region should be as high as possible and the graded region should be as narrow as possible, limited only by the requirement to flatten the quasi-Schottky barrier mentioned in the introduction. Theoretical investigations [9], presented in section 4.1, show that graded regions as narrow as 30nm should be permissible. In order to grow the compositional transition region, the Ga flux should decrease and the In flux increase simultaneously in a complementary, roughly linear fashion. At a given initial growth rate, the lower limit of the width of a graded transition region is given by the rate at which the Ga flux from the Ga effusion cell drops if the power to the latter is simply turned off. After some experimentation with the flux transient dynamics of the Ga and In sources, the following growth schedule was adopted. To facilitate the growth of graded transition regions as narrow as a few tens of nanometers, the overall growth rate was kept low, at 250nm/hr. During the growth of the GaAs layer, the indium furnace was kept idling at a reduced temperature that would correspond to a very low growth rate of about 2.5nm/hr, with the shutter closed. The growth of the transition layer was initiated by re-setting the indium furnace controller setpoint to the full 250nm/hr growth rate, and opening the shutter. After an additional 3min delay, the gallium furnace controller was reset to a 400°C idle temperature, and that furnace was simply allowed to cool. This caused the Ga flux to drop to approximately 1% of its initial value within ≈ 8 minutes. The overall thickness of the graded layer is estimated to be about 30nm. The doping level in the graded region and the InAs was about 3×10^{18} cm^{-3} .

For the p-type graded-gap contact structures a 200 nm p^+-GaAs buffer layer was grown first, followed by 30nm p^+-Ga(As,Sb) compositionally graded from GaAs to GaSb. The p^+-layers were doped with Be to about 5×10^{18} cm^{-3}. The antimony incorporation into a growing GaAs layer depends on the substrate temperature as well as the relative group V-to-group III flux ratios [11]. Consequently, the growth of the p-type graded gap contact required a slightly different approach than that for the n-type contacts. The growth of the graded region was initiated by opening the shutter of the Sb source.

Both the antimony-to-gallium and the initial arsenic-to-gallium atomic flux ratios were approximately 3 : 1. In the presence of such an arsenic flux at a substrate temperature of 600°C, very little (< 1%) antimony gets incorporated into the growing material [11]. During the growth of the graded region the substrate temperature was then ramped from 600°C to 470°C, for two reasons: (a) The temperature of congruent sublimation of GaSb is approximately 455°C [9] which is much lower than that of GaAs. Consequently GaSb requires a lower growth temperature than GaAs. (b) The substitution of arsenic by antimony is enhanced at lower growth temperatures [11], thus facilitating the growth of the graded layer. In addition, to accomplish a complete transition to GaSb, the power to the arsenic furnace was turned off 3 min into the growth of the graded region. The arsenic flux dropped to a tenth of its initial value at the end of the growth of the graded region, while the antimony flux remained constant.

4.4 Contact resistivity measurements

The specific contact resistivities of the n- and p- type graded-gap contacts were measured by the standard TLM method. For nonalloyed (Ga,In)As graded-gap contacts to n-GaAs, contact resistivities down to $5\times10^{-7}\Omega cm^2$ were obtained. For p-type Ga(As,Sb) graded-gap contacts, resistivities down to $3\times10^{-6}\Omega cm^2$ were measured.

For comparison, the typical values for Au/Ge/Ni n-type and Au/Zn p-type alloyed contacts found in the literature are $1\times10^{-6}\Omega cm^2$ [5] and $7\times10^{-6}\Omega cm^2$ [12]. While our resistivity values are competitive with those of typical n- and p- type alloyed contacts, it must be noted that they can be reduced even further by achieving higher doping levels in the graded layers. For instance, Nittono *et al.* have obtained contact resistivities as low as $5\times10^{-8}\Omega cm^2$ for layers graded to $Ga_{0.35}In_{0.65}As$ doped to $1.5\times10^{19}\ cm^{-3}$.

4.5 Heterostucture bipolar transistor with non-alloyed base and emitter contacts

It was decided to incorporate the graded-gap contacts into n-p-n AlGaAs/GaAs heterostructure bipolar transistors (HBTs). The advantages of having graded-gap contacts in a HBT are first the greatly reduced base and emitter contact resistances over those

possible with any conventional alloyed contacts. Besides, the graded-gap contacts are non-invasive. Therefore, thinner emitter structures will be possible since the ≈ 1000 Å penetration depth of the alloyed contacts need not be added to the emitter region thickness. Finally, the base and emitter metallizations can be performed in one step.

The HBT structure was grown by molecular beam epitaxy on a (100) oriented n^+-GaAs substrate. The doping, composition and thickness of the initial HBT layers are shown in Fig. 4.3. A 50nm Be-diffusion setback layer was used in the base [14]. The region between the base and the emitter was digitally graded with a narrow-well AlGaAs/GaAs superlattice as proposed by Su et al. [15]. The Al mole fraction in the (Al,Ga)As emitter was 0.25. The GaAs was grown at 600°C, and the (Al,Ga)As was grown at 650°C, with arsenic to group-III atomic flux ratios of approximately 2 : 1. The growth temperature was reduced to 600°C at the end of the emitter layer, and 30nm of (Al,Ga,In)As compositionally graded from (Al,Ga)As to InAs was grown, followed by 30nm of InAs, using a procedure similar to the one described for the growth of the (Ga,In)As graded-gap contact in section II. The graded region and the InAs were heavily doped n-type with Si to about $3\times10^{18}cm^{-3}$.

The sample was then removed from the MBE system and SiO_2 was deposited using plasma-enhanced chemical vapor deposition (PCVD) at 300°C. The SiO_2 was patterned into the emitter mesa regions using standard photoresist techniques. The SiO_2 was used as a mask for etching the emitter mesas, with $H_3PO_4 : H_2O_2 : H_2O = 4 : 1 : 50$. The sample was then rinsed in solvents, rinsed in de-ionized water for 10 min, cleaned in ozone for 10 min, and reloaded into the MBE system for the base contact regrowth. The various steps in the device fabrication sequence are shown in Fig.4.4.

The oxide was desorbed at approximately 620°C in an arsenic ambient. On samples that did not have the ozone cleaning mentioned above, the oxide desorbed at a lower temperature of about 600°C. We did not find a significant difference in samples grown with the ozone cleaning compared to those grown without. A small carbon peak was detected by Auger electron spectroscopy after the oxide desorption. Approximately 100nm of p^+-GaAs was grown to smooth out the restart interface. Then 30nm of p^+-Ga(As,Sb) compositionally graded from GaAs to GaSb was grown, followed by 30nm of p^+-GaSb,

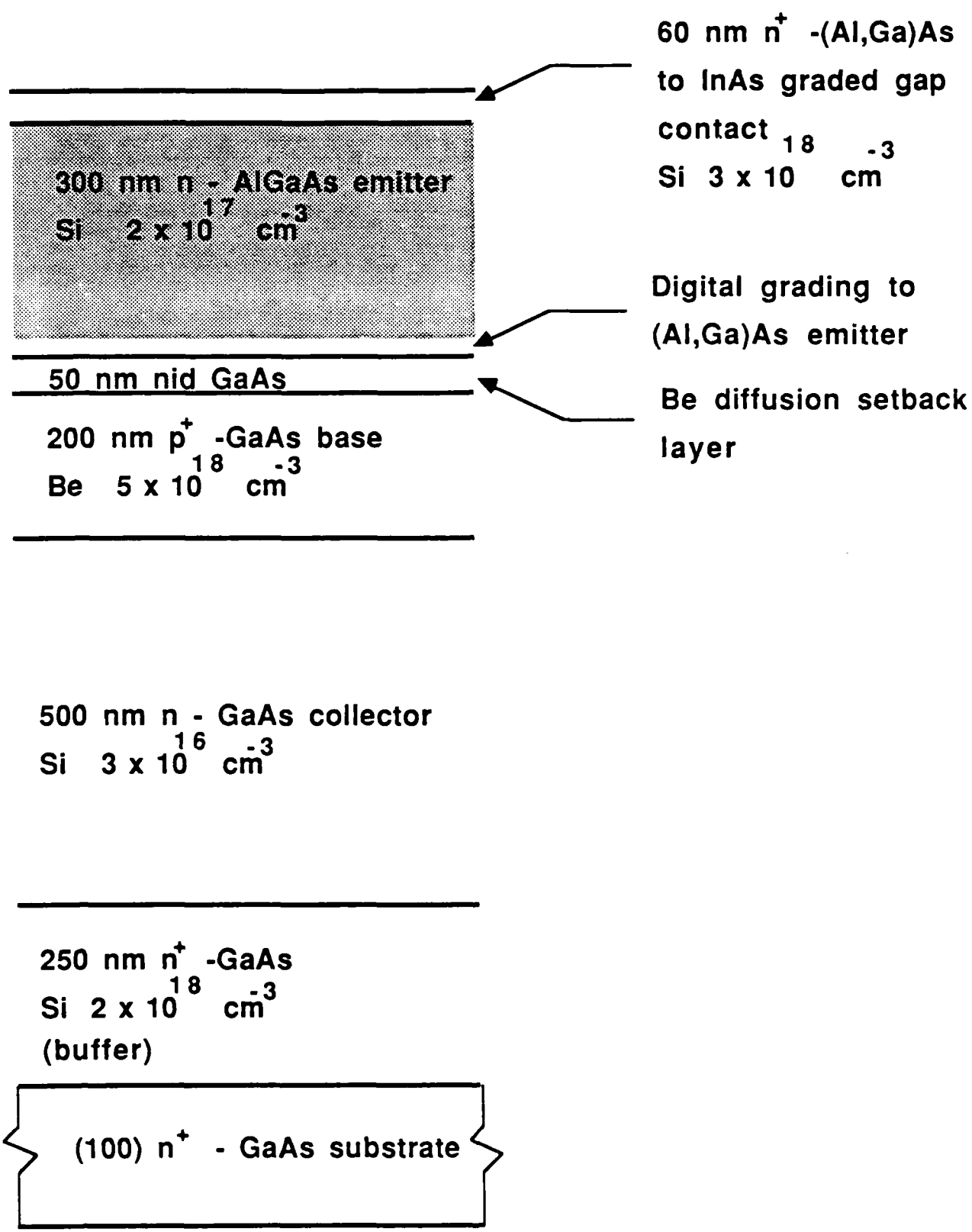


Fig. 4.3 Heterostructure bipolar transistor layer diagram. The structure was grown by MBE.

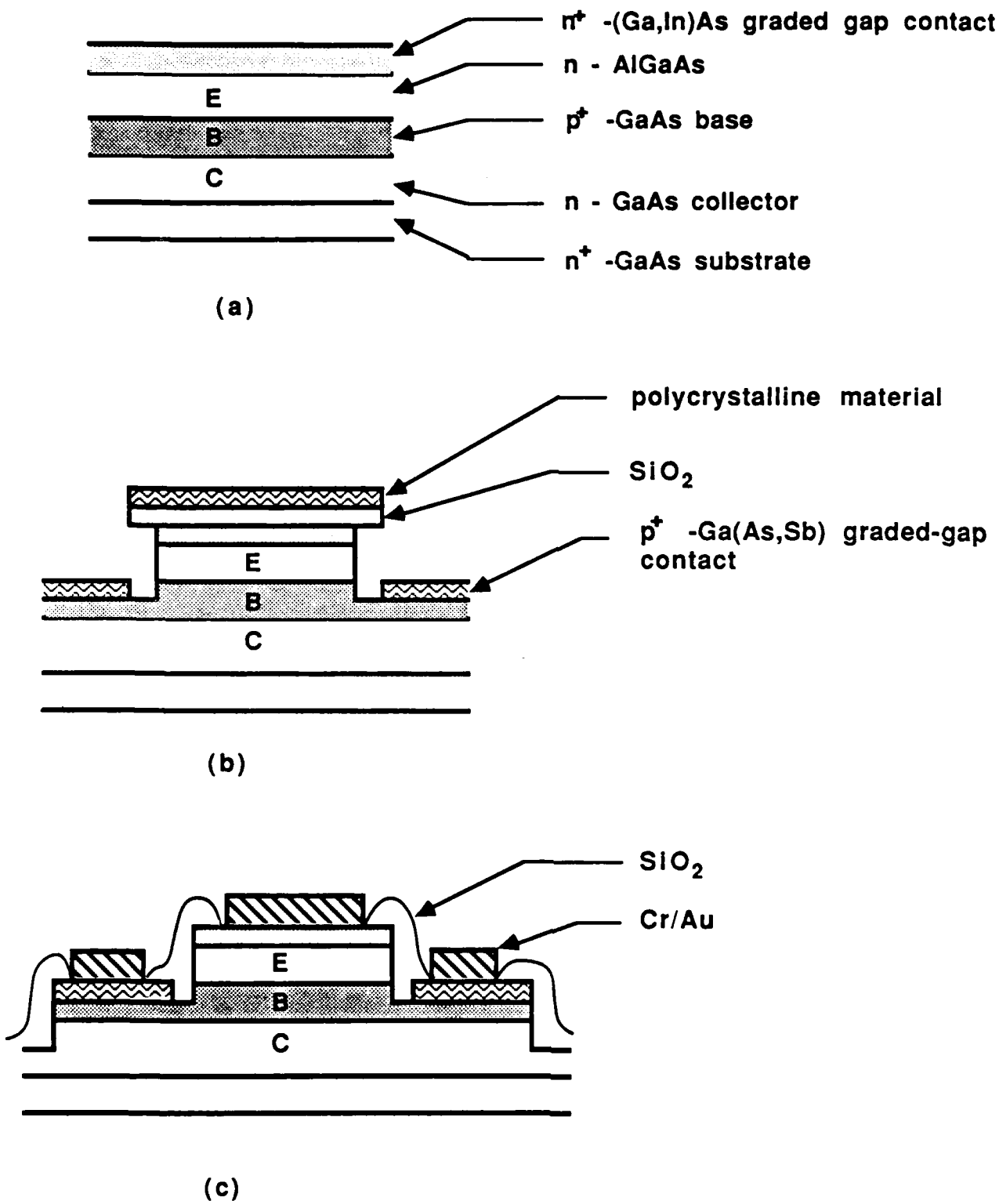


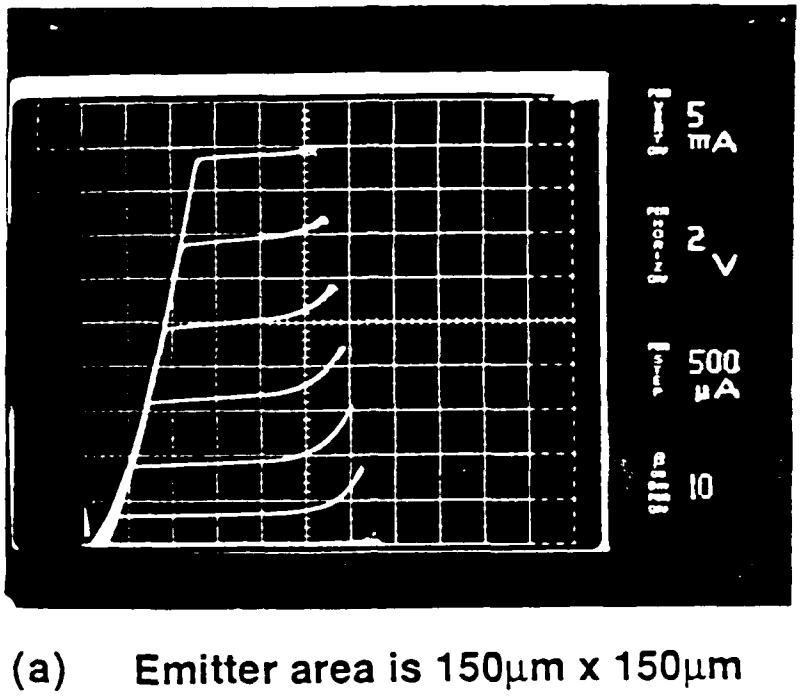
Fig. 4.4 Processing sequence for (Al,Ga)As/GaAs HBT with non-alloyed graded gap contacts.

as described in section 4.3. The doping in the p^+-layers was about 5×10^{18} cm^{-3}. Note that this MBE regrowth of the p-type contacts leads to base contact regions that are self-aligned with respect to the emitter mesas, a very desirable feature.

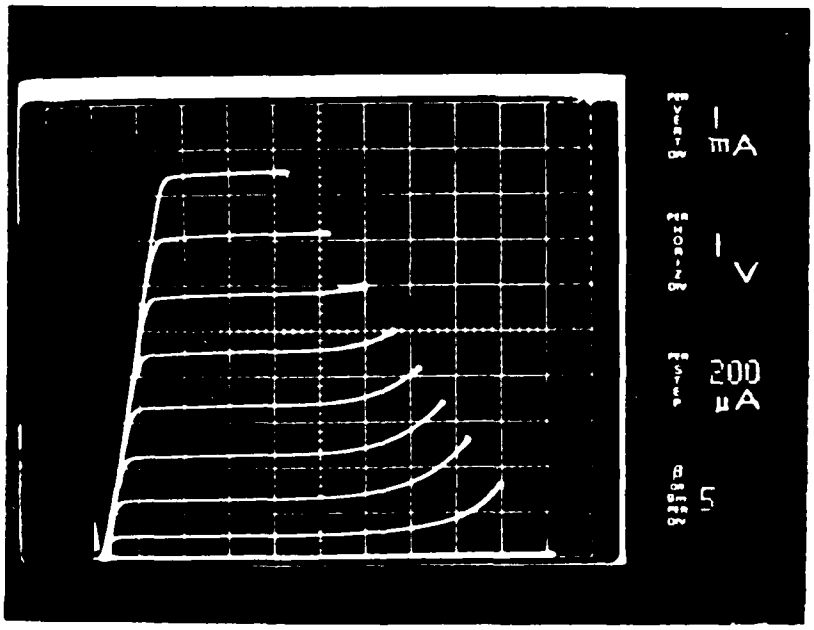
One of the potential advantages of graded-gap contacts is that they are capable of withstanding high temperature processing. Our growth procedure showed that the (Ga,In)As capped with SiO_2 could clearly withstand high temperatures of 620°C during the regrowth of the p-type graded-gap contact.

After the sample was removed from the MBE system the material grown on top of the SiO_2 was found to be polycrystalline and highly resistive. Furthermore, it appeared to be penetrated by an HF etch : the SiO_2 was easily etched off with HF, along with the material on top of the SiO_2. Base mesas were then etched, first using HF : H_2O_2 : H_2O = 10 : 1 : 100 to etch the Ga(As,Sb) and then using the phosphoric acid based etch mentioned above to etch the GaAs. At this point the device I/V characteristics could be obtained even prior to any final metallization, using tungsten probe tips to directly contact the semiconductor surfaces of the base and the emitter. Indium alloyed on the backside of the n^+-wafer formed the collector contact. Examples of I/V curves obtained in this manner are shown in Fig. 4.5(a).

In the next step, a dielectric (SiO_2) was deposited by PCVD, contact windows were cut and Cr/Au metallization was deposited by evaporation. Both the base and the emitter metallization were done in one step. No alloying was done. The device I/V curves obtained after final metallization is shown in Fig. 4.5(b). It should be noted that the I/V curves in Fig. 4.5(b) were obtained on devices fabricated in a different run than those corresponding to Fig. 4.5(a). It can be seen from the characteristics that the devices show no signs of excessive contact resistance. The I/V curves were very similar to those obtained on conventional alloyed contact transistors which were fabricated in a different run.



(a) Emitter area is 150µm x 150µm



(b) Emitter area is 20µm x 20µm

Fig. 4.5 Transistor I/V curves (a) obtained prior to metallization; (b) after final metallization. These transistors were from a different run than those corresponding to (a).

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5. SELF-ALIGNED HBT WITH GRADED-GAP CONTACTS.

5.1 Background

In the previous reporting period, we demonstrated the first (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT) that had non-alloyed graded-gap contacts to *both* the emitter and the base [1,2]. A n^+-graded (Ga,In)As layer was used as the emitter contact, and p^+-Ga(As,Sb) formed the base contact. Graded-gap ohmic contacts are now beginning to be incorporated in HBTs, as seen from other work appearing in literature. Self-aligned HBTs employing graded-gap contacts to only the emitter, with the emitter cap layer graded to $Ga_{0.5}In_{0.5}As$, have been reported [3,4]. Most recently, using such self-aligned HBTs, Nagata *et al.* [5] demonstrated ring oscillators that had a propagation delay of 5.5ps/gate, with the HBTs themselves having f_T's of 80 GHz and f_{max}'s of 60 GHz.

The contact resistivities of graded-gap contacts are competitive with those of alloyed contacts, and the nonalloyed contacts are non-invasive. They are, therefore, particularly attractive for HBTs, because emitter regions can be employed that are much thinner than those possible with alloyed contacts, leading to reduced emitter resistances. Also, the possibility of alloying through the thin base region is eliminated with nonalloyed base contacts. A further advantage of side-by-side incorporation of both n- and p-type graded-gap contacts into a HBT is that the base and emitter metallizations can be performed in one step, which makes it possible to fabricate self-aligned HBTs. The fabrication of such a self-aligned HBT is reported here.

5.2 MBE Growth of Graded-Gap Contacts and Contact Resistivity Measurements

Both n- and p-type graded-gap contacts were grown by molecular beam epitaxy (MBE) on (100)-oriented semi-insulating GaAs substrates for contact resistivity measurements. Our earlier report, and also [2], contains a description of the growth procedure, the salient features of which are as follows.

For the n-type graded-gap contact structures, approximately 200 nm of $1\times10^{18}cm^{-3}$

(Si-doped) n^+ -GaAs was grown at 600°C, followed by approximately 30 nm of n^+ -(Ga,In)As compositionally graded from GaAs to InAs. During the growth of the graded region, the substrate temperature was ramped down from 600°C to 500°C. Approximately 30 nm of n^+ -InAs was grown above the graded region. The doping level in the graded region and the InAs was about $3\times10^{18}cm^{-3}$.

For the p-type graded-gap contact structures, a 200 nm p^+ -GaAs buffer layer was grown first, followed by 30 nm p^+ -Ga(As,Sb) compositionally graded from GaAs to GaSb. The substrate temperature was ramped from 600°C to 470°C during the growth of the graded region. About 30 nm of p^+ -GaSb was grown above the graded layer. The p^+ -layers were doped with Be to about 5×10^{18} cm^{-3}.

The specific contact resistivities of the n- and p-type graded-gap contacts were measured by the standard TLM method. For nonalloyed (Ga,In)As graded-gap contacts to n-GaAs, contact resitivities down to 5×10^{-7} Ω cm^2 were obtained. For p-type Ga(As,Sb) graded-gap contacts, resistivities down to 3×10^{-6} Ω cm^2 were measured. While our resistivity values are competitive with those of typical n- and p-type alloyed contacts, it must be noted that they can be reduced even further by achieving higher doping levels in the graded layers. For instance, Nittono *et al.* [6] have obtained contact resistivities as low as 5×10^{-8} Ω cm^2 for layers graded to $Ga_{0.35}In_{0.65}As$ and doped to 1.5×10^{19} cm^{-3}.

5.3. Transistors

The HBT structure was grown by MBE on a (100)-oriented, semi-insulating GaAs substrate. The doping levels, compositions, and thicknesses of the initial HBT layers are shown in Fig. 5.1. The region between the base and emitter was graded from GaAs to (Al,Ga)As over 30nm. The Al mole fraction in the emitter was 0.3. The GaAs was grown at 600°C, and the (Al,Ga)As at 650°C with arsenic-to-group III *atomic* flux ratios of approximately 2:1. At the end of the emitter layer, 30 nm of n^+-(Al,Ga)As graded to GaAs was grown, and the growth temperature was reduced to 600°C. Then, the n^+-(Ga,In)As graded-gap contact layer was grown, as described in section 5.2 above.

The process sequence for the self-aligned HBTs is shown in Fig.5.2, and was as follows. The sample was removed from the MBE system and SiO_2 was deposited using

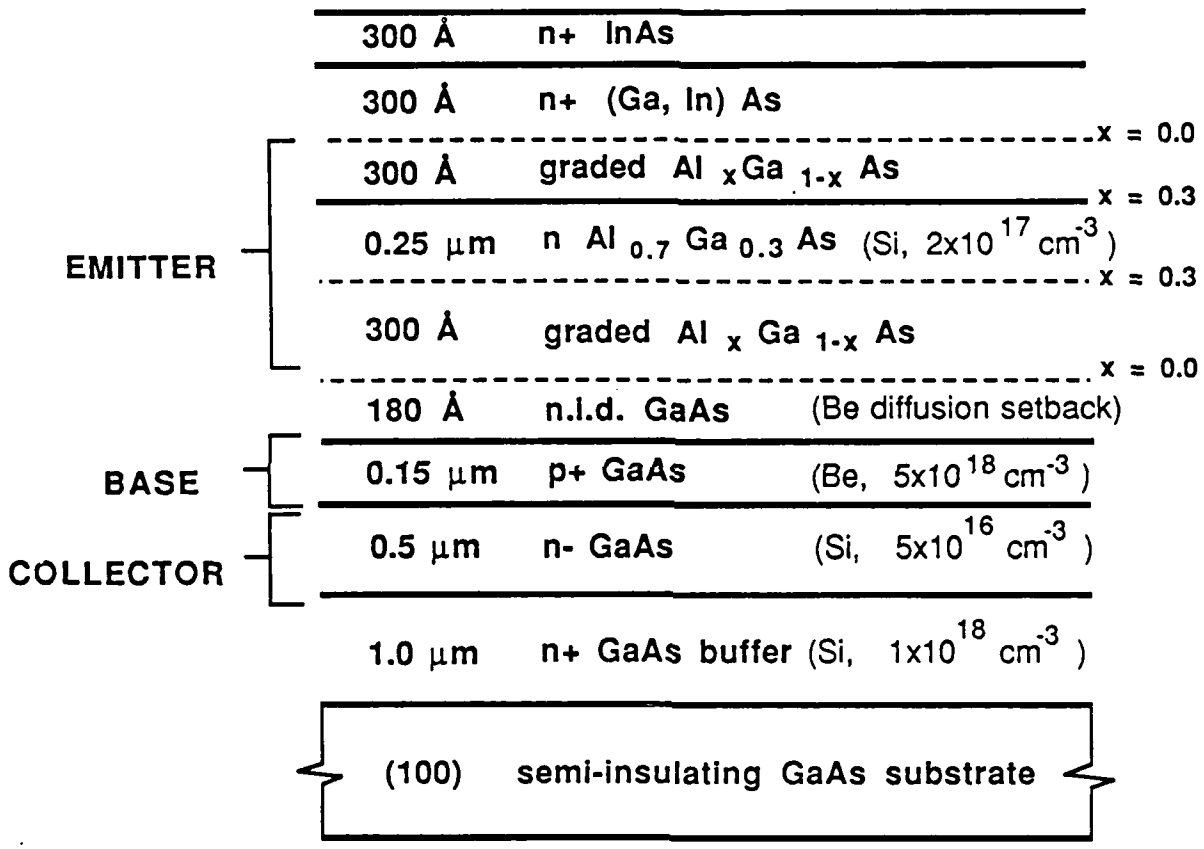


Fig. 5.1 AlGaAs/GaAs HBT layer diagram.

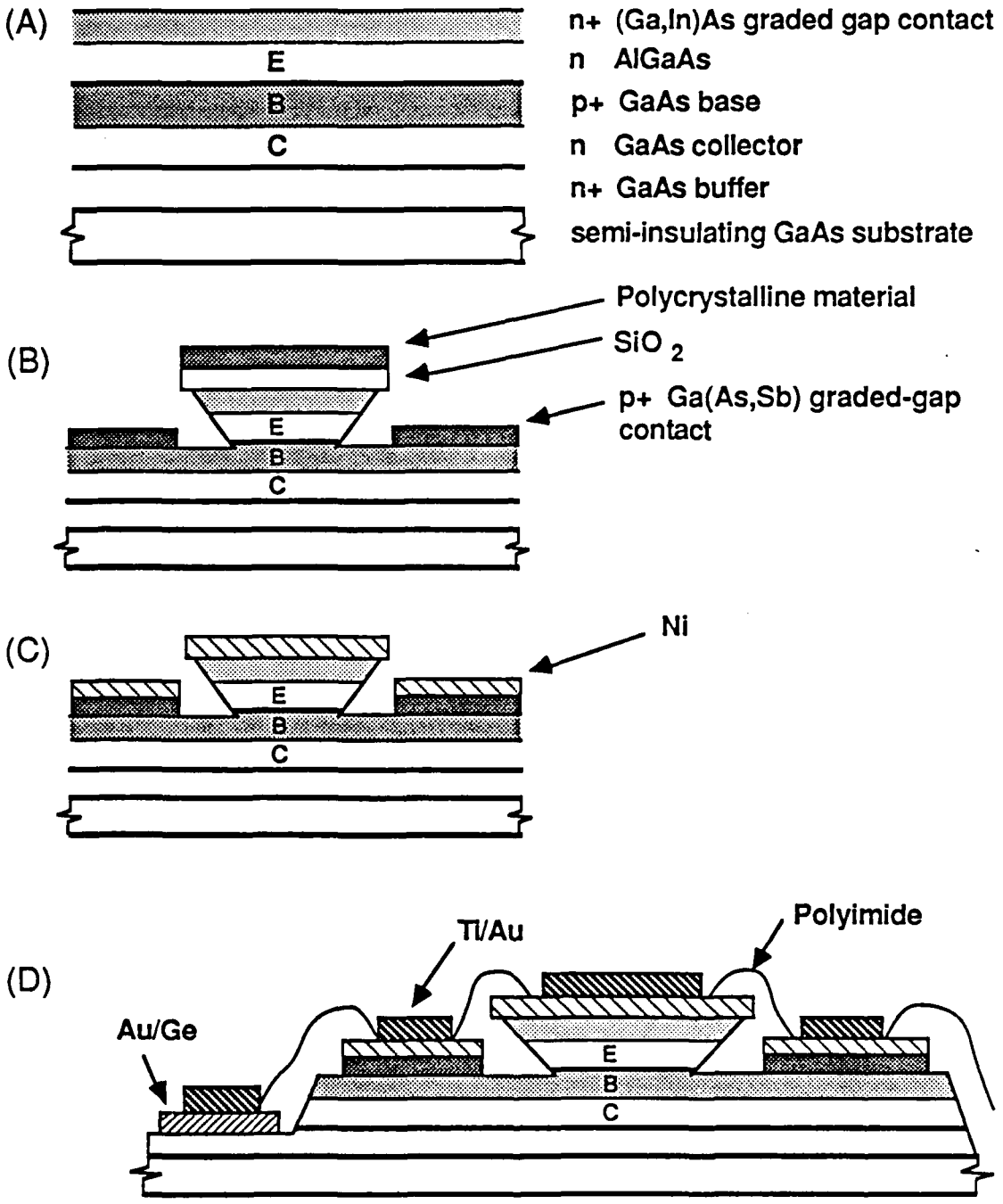


Fig. 5.2 Self-aligned HBT process sequence. (a) MBE grown structure; (b) emitter mesa etch followed by base regrowth; (c) self-aligned metal deposition, and (d) completed structure.

plasma-enhanced chemical vapor deposition (PCVD) at 300°C. The SiO_2 was patterned into the emitter mesa regions using standard photoresist techniques, and the emitter stripes were oriented so that they were parallel to the ⟨110⟩ direction of the crystal. The SiO_2 was used as a mask for etching the emitter mesas. The (Ga,In)As contact layer was etched with HCl, and the emitter mesa with $NH_4OH : H_2O_2 : H_2O$ (3 : 1 : 50). The NH_4OH based etch produced inward sloping sidewalls ("reverse-mesas") as reported by Fischer *et al* [7]. The sample was rinsed in deionized water for 10 min, and reloaded into the MBE system for base contact regrowth.

After desorption of the oxide at approximately 620°C in an arsenic ambient, 50nm of p^+ - GaAs was grown to smooth out the restart interface. The Ga(As,Sb) graded-gap contact was then grown as described in Section 5.2. During regrowth the SiO_2 acts as a cap for the n-(Ga,In)As contact and prevents its degradation. The overhang of the SiO_2 on the emitter mesa prevents growth on the sidewalls, and leads to Ga(As,Sb) regions that are self -aligned with the emitter mesas.

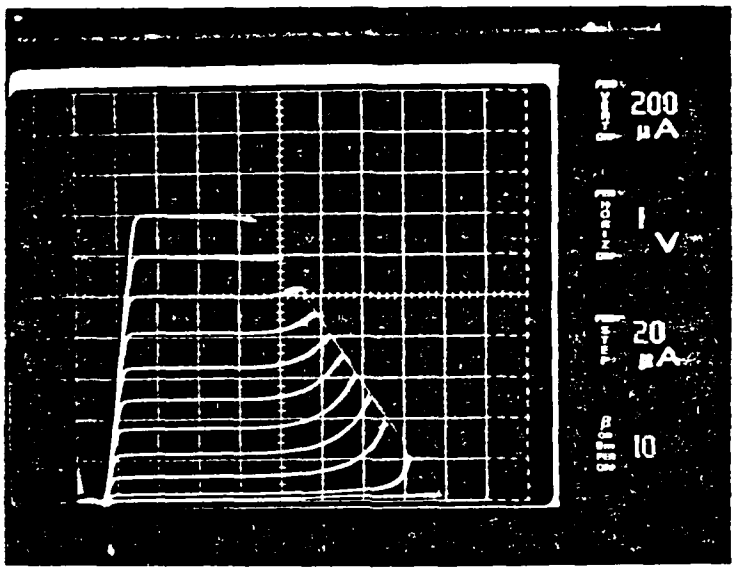
The regrown layer on top of the SiO_2 was removed by dissolving the SiO_2 in HF. Next, 40nm of Ni was deposited on the base and emitter surfaces. During metal deposition, the shadow created by the reverse-mesa prevents the base and emitter contacts from being shorted and leads to base contacts that are self-aligned with the emitter contacts. The separation between the regrown Ga(As,Sb) and the emitter mesa edge is determined by the undercut beneath the SiO_2 and is about 250nm. The separation between the base and emitter contact metal is much less than 250nm because this distance is determined by the shadow produced by the reverse mesa. After the base and collector mesas were etched, the collector contact was formed with alloyed Au-Ge/Ni/Au. Photosensitive polyimide was used as a dielectric, and final metallization was done with Ti/Au.

The device I/V curves obtained after final metallization are shown in Fig.5.3 The emitter stripe dimension was 7μm x 25μm, and the HBT had a current gain of 15 at collector current densities of about 15 kA/cm^2.

5.4. Calculated high frequency performance

High frequency characterization of the self-aligned HBT is in progress, and a

(a)



(b)

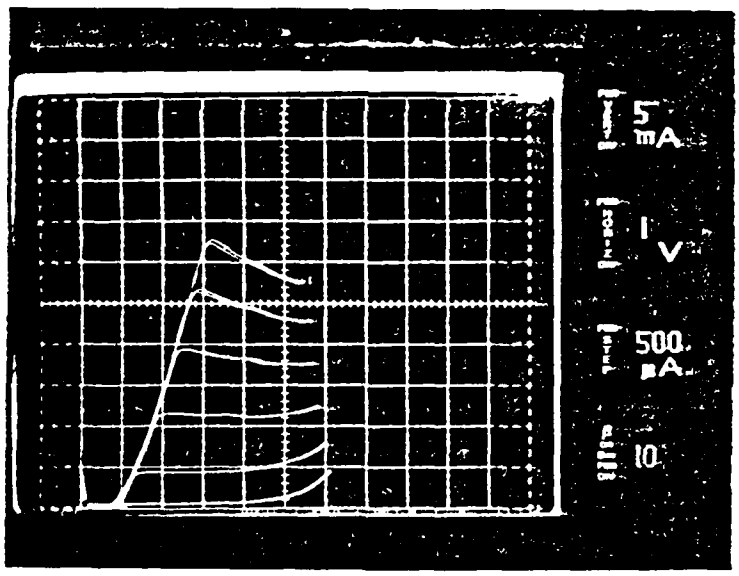


Fig. 5.3 I-V characteristics of the self-aligned HBT (emitter area = 7 μm x 25 μm) for (a) low and (b) high collector current densities.

performance estimate is presented here. For a base width of 0.15μm, base doping of $5\times10^{18}cm^{-3}$ and an assumed hole mobility of $100cm^2/Vsec$, the base sheet resistance is calculated to be 830 Ω/□. As mentioned in section III above, the self-aligned HBTs have a base-to-emitter contact separation of 0.25μm. The majority carriers must travel this distance, and an additional average distance 1/4 • W = 1.75μm under the emitter, W being the emitter width (7μm in the present case). The sides of the emitter total 50μm, and the base resistance is estimated to be 30Ω. For our device geometry, the base-collector area is approximately 20μm x 25μm, and the base-to-collector capacitance is calculated to be 0.17pF. Assuming an electron mobility of $1000cm^2/Vsec$ in the base, the base transit time is calculated to be 4.3ps. Using these values and the standard equations for the gain-bandwidth frequency (f_T), and the maximum frequency of oscillation (f_{max}) [8], the calculated f_T and f_{max} values for this device are : f_T = 37GHz and f_{max} = 17GHz. Improved device performance can be expected for emitter stripe widths narrower than 7μm, and for reduced base-to-collector areas.

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APPENDIX

Publications and presentations resulting from this research

Determination of valence and conduction-band discontinuities at the (Ga,In) P/GaAs heterojunction by *C-V* profiling

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The valence and conduction band discontinuities for the lattice matched (Ga,In)P/GaAs heterojunction have been determined by capacitance-voltage (*C-V*) profiling. Both *p-p* and *n-n* heterojunctions were profiled, in order to obtain separate and independent values for both the valence-band-edge discontinuity (ΔE_v) and the conduction-band discontinuity (ΔE_c). The band lineup is found to be of the straddling type with the valence- and conduction-band discontinuities 0.24 and 0.22 eV, respectively, with an estimated accuracy of $\pm$ 10 meV. Computer reconstruction of the *C-V* profiles was used to check the consistency of the data. The band offset data indicate that the (Ga,In)P/(Al,Ga)As system should be staggered for a certain range of Al compositions.

I. INTRODUCTION

The $Ga_{0.51}In_{0.49}P$/GaAs lattice-matched system has been proposed,[1] and recently demonstrated,[2] as an alternative to the (Al,Ga)As/GaAs system for *n-p-n* heterostructure bipolar transistors (HBTs). One reason that made the (Ga,In)P/GaAs system potentially attractive for *n-p-n* HBTs was the theoretical prediction,[1] based on Harrison's theory of band lineups,[3] that this system should have a larger fraction of the total energy-gap discontinuity occurring in the valence band than the (Al,Ga)As/GaAs system. An accurate experimental determination of the band lineup of the (Ga,In)P/GaAs system is therefore of interest. In the present paper, we report such a determination.

The method employed was capacitance-voltage (*C-V*) profiling through isotype heterojunctions, a technique introduced for determining band offsets at heterointerfaces by Kroemer *et al.*,[4] and recently employed with considerable success by several authors.[5–8] Both *p-p* and *n-n* heterojunctions were profiled, in order to obtain separate and *independent* values for both the valence-band-edge discontinuity (ΔE_v) and the conduction-band discontinuity (ΔE_c), to permit the powerful self-consistency check of whether or not the values of the two discontinuities add up to the known energy-gap difference (ΔE_g) between the two materials, as in the work of Watanabe *et al.*[8]

An additional check was performed, by comparing the actual experimental profiles with computer reconstructions of what the *C-V* profiles *should have been* for the particular band offset data found, *if* the heterojunctions satisfied the simple theoretical model of a perfectly abrupt junction.

II. SAMPLE PREPARATION

A. Sample structures

Epitaxial layers of (Ga,In)P and GaAs were grown by molecular beam epitaxy in a Varian-360 MBE machine, on (100)-oriented, Si-doped n^+-GaAs substrates. Both *n-n* and *p-p* isotype structures were grown, for separate ΔE_c and ΔE_v measurements. The overall structures, with the thicknesses and doping levels of the layers, were as shown in Fig. 1. With the *n-n* structures, the profiling was conducted from a reverse-biased aluminum Schottky barrier deposited on the *n*-(Ga,In)P surface [Fig. 1(a)]. Because Schottky barriers on *p*-(Ga,In)P were too leaky to permit *C-V* profiling, the profiling of the *p-p* heterojunctions (HJs) was carried out by continuing to use an n^+ substrate, and profiling upward from the reverse-biased n^+-*p* junction between the substrate and the *p*-GaAs epilayer [Fig. 1(b)]. The schematic energy-

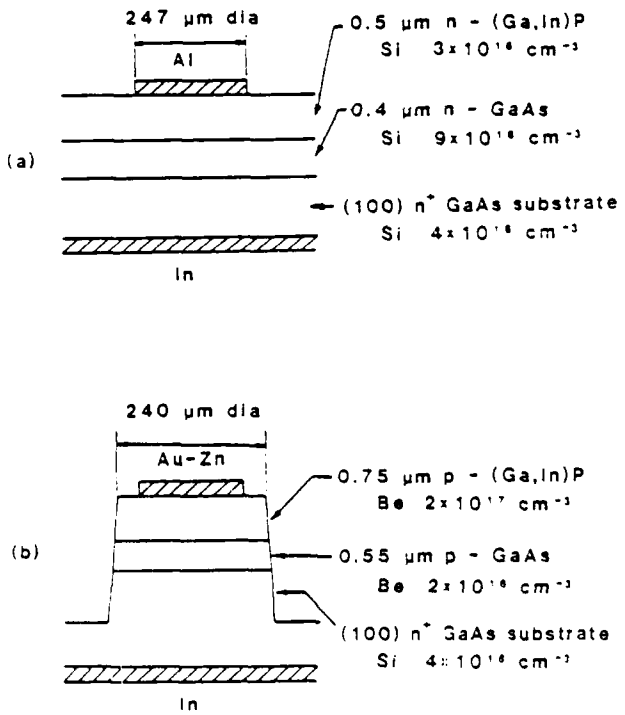

FIG. 1. Structure of samples for *C-V* profiling: sample for determination of (a) conduction-band offset by profiling through an *n-n* junction from a surface Schottky barrier; (b) valence-band offset by profiling through a *p-p* junction from a buried n^+-*p* junction.

[a] Now at GEC Hirst Research Center, Wembley, Middlesex, England.
[b] Now at Avantek Inc., Santa Clara, CA 95051.

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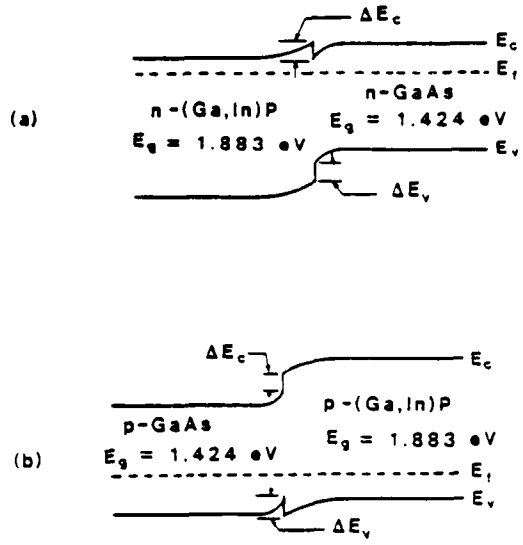

FIG. 2. Expected band diagrams for the (a) *n-n* heterojunction; (b) *p-p* heterojunction. Both are oriented such that the profiling direction is from the left to the right.

band diagrams of the HJ portion of the two structures are shown in Fig. 2, both oriented such that the profiling direction is from the left to the right.

B. Growth procedure

The GaAs substrates were cleaned in organic solvents, and etched in $NH_4OH:H_2O_2:H_2O = 2:1:20$ at room temperature for 2 min. This was followed by a 10-min rinse in deionized water to form a native oxide. The oxide was desorbed by heating inside the MBE system at a substrate temperature of 600 °C in the presence of an As_2 arsenic flux for 7 min, until a streaky 2×4 surface reconstruction was observed via reflection high energy electron diffraction (RHEED). The GaAs epilayers were grown at 605 °C, at a growth rate of 0.35 μm/h. The arsenic-to-gallium *atomic* flux ratio ($=2As_2$:Ga) was approximately 3:1. After the growth of the GaAs epilayer, the As_2 source was turned off and the P_2 phosphorus source was heated up. This changeover took approximately 45 min. The P_2 source was a GaP decomposition source equipped with a special baffle to condense out any residual Ga in the P_2 beam.[9] The differential P_2 pressure at the substrate position was measured by a nude ionization gauge to be about 8×10^{-6} Torr. The (Ga,In)P epilayers were nucleated at a substrate temperature of 505 °C, using a growth rate of 0.7 μm/h. The RHEED pattern was streaked, with a 2×4 reconstruction, throughout the growth of the (Ga,In)P epilayers. The morphology of the epilayers was mirror smooth under interference contrast optical microscopy.

One of the central problems in the MBE growth of ternary alloy semiconductors is the achievement of an alloy composition with good lattice match at the HJ. This requires a careful control of the Ga:In flux ratio. Our nude ion gauge beam flux monitor was found to be insufficiently reproducible to obtain the desired lattice match reliably. Therefore, x-ray diffractometer data were taken on all layers grown, and layers with unsatisfactory lattice match were discarded. On our best *n-n* sample, diffractometry indicated that the (Ga,In)P epilayer was slightly Ga rich with a relative lattice mismatch of approximately 10^{-3}, while on our best *p-p* sample a much smaller relative lattice mismatch of less than 10^{-4} was achieved. These were the two samples on which detailed *C-V* profiling studies were performed, reported here.

C. Preparation of samples for *C-V* profiling

On the *n-n* samples, aluminum Schottky barriers were fabricated by deposition and liftoff. The diode area was 4.8×10^{-4} cm^2. On the *p-p* samples, Au–Zn dots were deposited by evaporation and liftoff, and alloyed at 450 °C for 30 s on a graphite strip heater, to form an Ohmic contact to the *p*-(Ga,In)P. Diode mesas were then formed by etching the (Ga,In)P with $HCl:H_3PO_4 = 1:1$. We found that this etchant produced less undercutting than the undiluted HCl etch commonly used for etching (Ga,In)P. Following the (Ga,In)P etch, the *p*-GaAs was etched with $H_3PO_4:H_2O_2:H_2O = 5:1:14$, to a depth sufficient to reach into the n^+ substrate. The final *p-p* diode mesa area was measured to be 4.6×10^{-4} cm^2. The return contact for both *n-n* and *p-p* structures was formed by indium alloyed to the n^+ substrate.

III. *C-V* PROFILING: RESULTS AND DISCUSSION

A. ΔE_v measurements

Because we found the *p-p* results more trustworthy, they are discussed first.

As stated earlier, the *C-V* profile through the *p*-(Ga,In)P/*p*-GaAs HJ was obtained by reverse biasing the n^+-*p* junction between the substrate and the *p*-GaAs epilayer, shown in Fig. 1(b). A HP4280A *C-V* meter was used for the measurement. The measurement frequency was 1 MHz, and the magnitude of the applied differential voltage was 30 mV (rms). The *apparent* majority carrier concentration profile $p^*(x)$ was derived from the *C-V* profile according to the standard relation

$$p^*(x) = \frac{2}{q\epsilon}\left(\frac{d}{dV}\,\frac{1}{C^2}\right)^{-1}, \tag{1}$$

where

$$x = \epsilon/C \tag{2}$$

is the width of the depletion layer, essentially the distance of the depletion layer edge from the *p-n* junction. The various symbols in Eqs. (1) and (2) have the following meanings:

$p^*(x)$: apparent majority-carrier (hole) concentration at position x;

V: reverse bias voltage;

C: capacitance per unit area;

ϵ: dielectric permittivity of the semiconductor.[10]

An experimental apparent carrier concentration profile is shown as a solid line in Fig. 3. Hole accumulation is seen in the GaAs, and a depletion region in the (Ga,In)P, as expected from the band diagram of Fig. 2(b). The doping in the n^+ substrate, 4×10^{18} cm^{-3}, was sufficiently large that the correction to the profile due to a small amount of depletion into the substrate could be neglected. Also shown in Fig. 3, as a broken curve, is a "best fit" computer-generated theo-

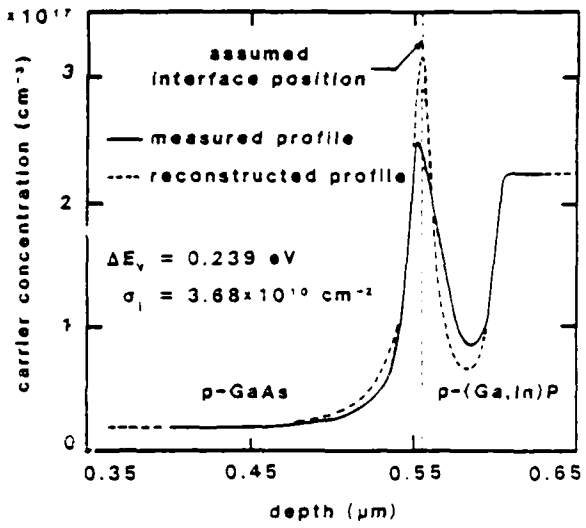

FIG. 3. Experimental and reconstructed apparent carrier concentration profiles for the *p-p* structure.

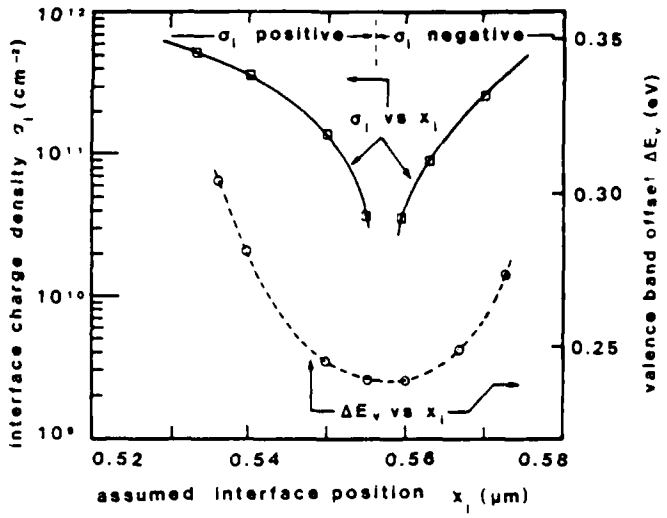

FIG. 4. Plot of the valence-band offset ΔE_v and interface charge σ_i for the *p-p* heterojunction, as a function of assumed interface position x_i.

retical $p^*(x)$ profile, which will be discussed later.

The value of ΔE_v is obtained from the electrostatic dipole moment associated with the charge imbalance between a presumably known doping distribution $P(x)$ and the experimental $p^*(x)$ curve, using the relation given by Kroemer *et al.*,[4] adapted to the *p-p* case:

$$\Delta E_v = \frac{q^2}{\epsilon}\int_0^\infty [P(x) - p^*(x)](x - x_i)dx - kT\ \ln\left(\frac{P_2 N_{v1}}{P_1 N_{v2}}\right). \tag{3}$$

Here the newly introduced symbols have the following meanings:

ΔE_v: valence-band-edge discontinuity, counted positive if the step is upward when going from the (Ga,In)P towards the (GaAs), as assumed in Fig. 2(b);

$P(x)$: ionized acceptor distribution, assumed to be known and to level out far away from the HJ;

$P_{1,2}$: asymptotic values of the doping levels in the GaAs (#1) and the (Ga,In)P(#2);

x_i: distance of the HJ interface from the n^+-*p* junction;

$N_{v1,2}$: valence-band density of states in the two regions.

An accurate determination of P_1 and P_2 is necessary if the band discontinuity is to be obtained with confidence. It can be seen from the $p^*(x)$ curve that the hole concentrations on both sides of the HJ leveled out very well; thus P_1 and P_2 could be established accurately.

To evaluate Eq. (3), we assumed a model of uniform doping on both sides of the interface plane $x = x_i$, with an abrupt step in the doping at $x = x_i$, as well as the existence of a localized interface defect charge σ_i at $x = x_i$. For a given value of x_i, the value of σ_i is obtained from the requirement of overall charge neutrality[4]:

$$\sigma_i = \int_0^\infty [p^*(x) - P(x)]dx. \tag{4}$$

In such a model an accurate knowledge of the interface position x_i is essential. Although a *nominal* value of the thickness of the GaAs layer was known from the growth rate, the accuracy of this value was not sufficient for use in reliably determining ΔE_v, and the value of x_i had to be determined, as usual, from the profile itself. To this end a *series* of values of ΔE_v and of the interface charge density σ_i were calculated from Eqs. (3) and (4), for a series of *assumed* values of the interface position x_i around the neutral value, leading to the results in Fig. 4. It is evident that the valence-band offset ΔE_v exhibits a broad minimum around that x_i value that corresponds to zero interface charge. This minimum is an inherent property of the model: It is not difficult to prove[11] that such an interpretation in terms of a step profile model always leads to an extremum of the band offset at that assumed x_i value for which the interface charge vanishes (a maximum or minimum, depending on the signs of the band offset and of the doping step). For HJs with a low *true* interface charge this behavior has the beneficial consequence that the calculated band offset value is a relatively insensitive function of the assumed interface location, and for such junctions one may, to the first order, determine the band offset by simply choosing for x_i that value for which $\sigma_i = 0$. For our sample this procedure yielded a valence-band offset $\Delta E_v = 0.238$ eV.

However, in the absence of additional evidence, the above procedure gives no assurance that the interface defect charge is in fact small enough, or even that the model of an abrupt doping step plus interface charge is applicable at all. We therefore performed the additional check mentioned in Sec. I of a computer reconstruction of what the $p^*(x)$ profile *should have been* for an abrupt junction with given values of band offset and interface charge, using a computer program that basically solves Poisson's equation for incremental voltage steps applied to the HJ.[12] Such a computer reconstruction proved useful in our earlier work,[4] and more recently it was used with excellent success by Watanabe *et al.*[5]

Specifically, we calculated values of ΔE_v and σ_i from the experimental $p^*(x)$ profile for a range of assumed values of x_i, and used them to reconstruct numerically the apparent carrier concentration profiles associated with the different

sets of values. These were then compared with the experimental profile for each of the assumed x_i values, as in the work of Watanabe *et al.*.[8] The broken curve in Fig. 3 shows the best overall fit that could be obtained for our *p-p* junction, for $x_i = 0.555\ \mu$m, yielding $\Delta E_v = 0.239$ eV and $\sigma_i = +3.68\times10^{10}$ cm^{-2} near the band offset minimum in Fig. 4, but not exactly at it. Note that the change in band offset from the value at the minimum is only 1 meV. Although we were unable to obtain as close a fit as in the better samples of the work of Watanabe *et al.*,[8] or of our own earlier work[4] on (Al,Ga)As/GaAs, the agreement between the experimental and reconstructed profiles is quite good. The remaining discrepancies must be viewed either as due to experimental errors, or as indications that our model of a perfectly abrupt interface is not fully applicable, but it is difficult to say more.

Expressed as a fraction of the known total energy-gap difference, $\Delta E_g \approx 0.459$ eV,[13] our ΔE_v value corresponds to $0.52\ \Delta E_g$. This value is about 50 meV smaller than the originally predicted $\Delta E_v \approx 0.29$ eV $\approx 0.63\ \Delta E_g$ for the lattice-matched $Ga_{0.51}In_{0.49}P$/GaAs interface, obtained by simple linear interpolation[1] between the theoretical valence-band offsets for GaP/GaAs and InP/GaAs predicted by the Harrision theory.[3] Although not negligible, this descrepancy is actually smaller than that between experiment and prediction from the Harrison theory for most heterosystems.

B. ΔE_c measurements

The structure shown in Fig. 1(a) was used to measure ΔE_c. The aluminum Schottky barrier was reverse biased to obtain a *C-V* profile through the HJ. The analysis of the data was analogous to that for the *p-p* structure. Figure 5 shows the experimental carrier concentration profile, in which electron accumulation and depletion can be seen in the GaAs and (Ga,In)P, again as expected from the predicted energy-band diagram shown in Fig. 2(a). Figure 6 shows a graph of ΔE_c and σ_i as a function of x_i. Note that this time

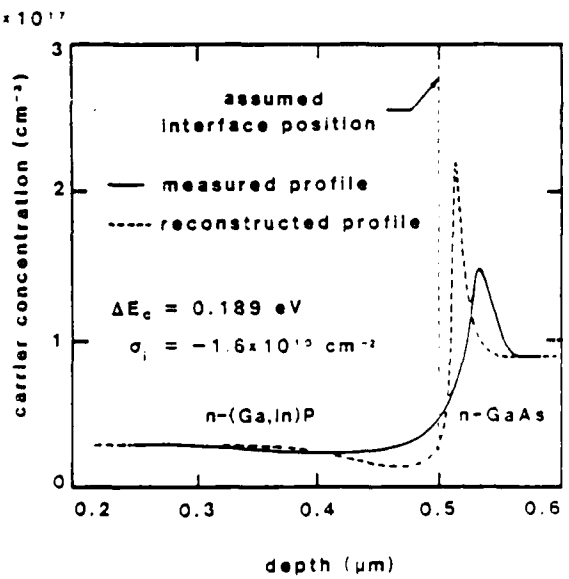

FIG. 5. Experimental and reconstructed apparent carrier concentration profiles for the *n-n* structure.

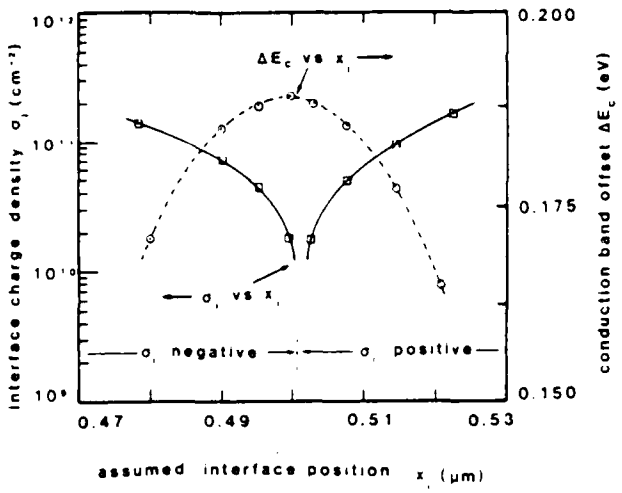

FIG. 6. Graph of conduction-band offset ΔE_c and interface charge σ_i for the *n-n* heterojunction as a function of assumed interface position x_i.

the band of offset extremum is a maximum.

We were not able to obtain a good fit between experimental and reconstructed carrier concentration profiles. The reconstructed profile shown in Fig. 5 represents the "least bad" fit, corresponding to the triplet $x_i = 0.500\ \mu$m, $\Delta E_c = 0.189$ eV, $\sigma_i = -1.6\times10^{10}$ cm^{-2}. Again this profile is one with a small interface charge, and again the value of the band offset is not very sensitive to the choice of x_i. But the peak-to-valley concentration ratio of the experimental profile is lower, and the peak and valley are separated farther in space than in the reconstructed profile. This combination indicates that the ionized impurity profile and/or the energy gap of the actual junction must be graded at the transition, in contrast to the mathematical model used in the reconstruction, which assumed an abrupt transition at the interface for both. MBE-grown junctions tend to be compositionally quite abrupt,[14] and it would in fact be difficult to explain an unintentional compositional grading wide enough to explain the discrepancy between the two curves in Fig. 5, but impurity diffusion or carryover could easily have taken place. If one inspects the *n-n* equivalent of Eq. (3) for our case of a heavier doping on the GaAs side, one finds readily that the presence of a doping gradient at the interface causes an *increase* in the value of ΔE_c relative to the abrupt-model value. In fact, our raw band offset data add up only to $\Delta E_v + \Delta E_c = 0.428$ eV, a value 31 meV smaller than the *known* energy-gap difference $\Delta E_g \approx 0.459$ eV, a discrepancy of about 7%, giving further credence to the assumption of a graded impurity profile.

To estimate the effect of grading on the calculated band offset value, at least to a first order, the doping gradient may be approximated by a straight line, with a half-width equal to the distance between the accumulation and depletion extrema in the experimental profile, as shown in Fig. 7. The contribution of the grading to the electrostatic dipole moment would then be simply that of the two shaded triangles, about 24 meV, within 7 meV of the band offset sum discrepancy of 31 meV. A gradient only 14% wider would have yielded the full discrepancy. Although the estimate is crude, it is clear that the correction is quite close to the discrepancy,

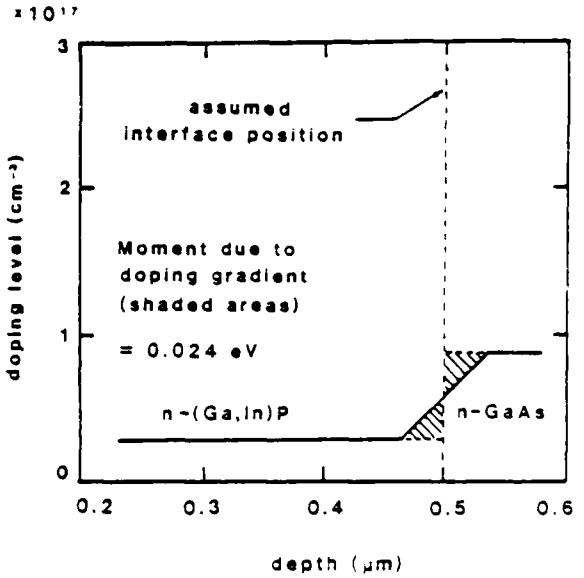

FIG. 7. Simple model for the doping gradient postulated to be present in the *n-n* heterojunction.

lending strong support to the hypothesis that most of the discrepancy is due to grading of the ionized impurity concentration. A more accurate check would have been a computer reconstruction using a graded profile with a more realistic graded profile, but we currently do not have a suitable computer program for such more advanced reconstructions.

Presumably, some grading might also be present at the *p-p* junctions, but the amount is clearly much smaller, and any correction to the valence-band offset would be quadratically smaller. Within the accuracy of our data we may therefore allocate the entire discrepancy to the conduction-band offset, yielding a corrected conduction-band offset of $\Delta E_c \simeq 0.22$ eV $\simeq 0.48 \Delta E_g$. The value of ΔE_c predicted from the Harrison model was 0.160 eV $\simeq 0.35 \Delta E_g$.

The origin of the postulated impurity gradient is not clear, but we suspect that it might be due to strain-induced diffusion: Studies of masked diffusion in GaAs[15] have shown the presence of large lateral diffusion of the diffusant in the presence of strain at the mask/GaAs interface. In those studies the masks were deposited films of silica, phosphosilicate glass, or silicon nitride, and the strain at the mask/GaAs interface was due to their different thermal expansion characteristics. In our *n-n* sample, significant out-diffusion of Si could have taken place at the GaAs/(Ga,In)P interface, due to strain caused by the non-negligible residual lattice mismatch in that sample. In contrast, it should be recalled that *p-p* isotype interface was relatively strain free.

A comment is in order concerning the possibility that in addition to the impurity gradient there might be a gradient in the energy gap present. The *n-n* equivalent of Eq. (3) was originally derived in the case that the energy gap changes abruptly. It was subsequently shown[16] that the relation remains valid if the energy gap is graded, so long as the correct ionized impurity distribution is known and used in the evaluation of Eq. (3). In this case the band offset derived from Eq. (3) is always that offset which would have been present *if* the junction had been abrupt. The energy-gap variation does not enter the problem of offset determination; only a knowledge of the ionized impurity concentration $P(x)$— or $N(x)$— as function of position is required. However, in the presence of energy-gap grading, the reconstruction of the apparent carrier concentration profile will fail, even if performed with correct values of the offset and the ionized impurity profile. For example, in the (unlikely) limit of a gradient in the energy gap alone, unaccompanied by a doping gradient, the experimental apparent electron concentration profile would be spread out, and hence would lead to a failure of the reconstruction of this profile using an abrupt model. But in evaluating the conduction-band offset from the *n-n* analog of Eq. (3), the effects of profile lowering and profile spreading would cancel out exactly,[16] yielding the band offset value of the ungraded junction.

C. Comments on possible sources of errors

It is difficult to place an exact error estimate on our band offset values. The largest single source of uncertainty is the quality of our samples. Although *C-V* profiling is potentially a powerful and accurate method, its success depends far more on the quality of the samples than the published literature on the subject suggests. While we would have preferred to have samples of a quality approaching that of the (Al,Ga)As/GaAs HJ samples reported in the literature, that option was not available, given the state of the technology for the MBE growth of reasonably abrupt, well lattice-matched (GaIn)P/GaAs HJs. In fact, the measurements reported here were themselves part of the early phases of the development of such a technology. Our *p-p* sample is clearly the better of the two samples, even if one ignores the evidence provided by the computer reconstructions of the two profiles: It has less lattice mismatch, and the *C-V* profile itself has a much more pronounced peak-and-valley structure, suggesting much less trouble from grading and from interface charge effects. However, without computer reconstruction it would be difficult to be more specific and to give an error estimate. The reconstruction fit, although far from perfect, is much better than for the *n-n* sample, suggesting that any errors due to impurity grading effects are much smaller than our earlier estimate of 20–30 meV for the grading correction in the *n-n* case, certainly below $\pm$ 10 meV.

The principal potential source of any larger error could be deep levels at or near the interface, including, but not restricted to deep levels associated with misfit dislocations. By deep levels we mean here levels whose ionization changes with changing bias. Their effect on the apparent carrier concentration profile is at this time not understood, and conceivably they might introduce changes into the interpretation of these profiles that would lead to changes in the band offsets larger than our otherwise conservative error estimate for the *p-p* junctions. An investigation of such effects was beyond the scope of our work, and in the absence of any other evidence of such changes we believe that ignoring them is justified, at least for the *p-p* junctions.

Considering that we are quoting band lineups on the millivolt level, less than 2%–3% of the overall energy gap difference, one natural area of concern is the extent to which

: capacitance measurements themselves are accurate ɔugh. Practical experience with the accuracy of *C-V* pro- ng in determining doping profiles might suggest that such :uracies are illusory. Surprisingly, however, many mea- :ement errors that would lead to incorrect doping profiles ıcel out in band offset determinations. Any error in the ɔacitance measurements by a *constant* factor, e.g., by an or in the diode area, cancels out of the band offsets: Al- ɔugh such an error would yield an incorrect apparent car- r concentration, it also yields an incorrect position allo- ted to this carrier concentration, and the two errors cancel *ıctly* when the band offset is calculated![17] Furthermore, :n certain kinds of nonconstant errors cancel out: It has en shown[10,12] that the permittivities of both semiconduc- :s cancel out of the band offset, even if the two permittivi- s are different. Hence any measurement error mathemat- ılly equivalent to an error in the two permittivities cancels t.

. CONCLUSION

The valence- and conduction-band-edge discontinuities : (Ga,In)P lattice matched to GaAs have been determined *C-V* profiling. As expected, the band lineup between ɔa,In)P and GaAs is of the straddling type. Reasonable reement between the experimental and reconstructed pro- :s was obtained for the *p-p* isotype structure, and the va- ıce-band discontinuity was obtained to be 0.24 eV, or 52ΔE_g. Comparison of the experimental and reconstruct- profiles for the *n-n* isotype structure indicated the pres- ce of significant grading at the interface. A first-order cor- :tion of the raw data to the measured ΔE_c was estimated, :lding a corrected value of ΔE_c of 0.21 eV, or 0.46 ΔE_g. :ese values of ΔE_v and ΔE_c, obtained from independent easurements, add up to 98% of ΔE_g, indicating good self- nsistency, and suggesting an accuracy of the individual lues themselves to probably better than $\pm$ 10 meV. Be- use the grading correction for the *n-n* junction was based a rather crude estimate, and because the two band offsets *ust* add up to the known energy-gap difference, we allocate e remaining 7-meV discrepancy to the conduction-band set, leading to a final value of ΔE_c of 0.22 eV, or 0.48ΔE_g.

Our lineup data lead to interesting predictions for the nd lineups for (Ga,In)P lattice matched to $Al_xGa_{1-x}As$. Fig. 8, taken from a recent review,[18] we have superim- sed our conduction- and valence-band-edge energy values : (Ga,In)P on current "best estimate values" for the lin- ps *within* the $Al_xGa_{1-x}As$ alloy system.[18] It appears that : valence band of $Al_xGa_{1-x}As$ will drop below that of tice-matched (Ga,In)P for $x > 0.47$. The conduction- nd offsets are more complicated, due to the Γ-to-X cross- er in the $Al_xGa_{1-x}As$ band structure around $x = 0.43$. e estimate that the conduction band of $Al_xGa_{1-x}As$ will e initially above that of (Ga,In)P for $x > 0.27$. For >0.43, the conduction-band energy of $Al_xGa_{1-x}As$ ɔps again, and it should reach a valley very close to the ia,In)P value as $x \to 1.0$. Thus there are likely to be three $_xGa_{1-x}As$ composition ranges with quite different be- vior: (i) For $x < 0.27$, the band lineup should remain a addling one, with $Al_xGa_{1-x}As$ retaining the lower total p, and with a vanishing conduction-band offset at the up-

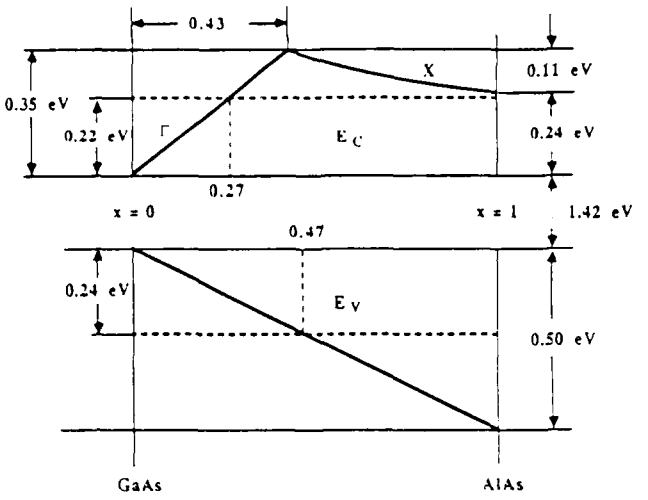

FIG. 8. Predicted relative band-edge energies at (Ga,In)P/(Al,Ga)As. The heavy solid lines represents the band-edge energies in the alloy system, relative to straight GaAs, as a function of x, taken for Ref. 18. The horizontal broken lines represent the (Ga,In)P band energies relative to GaAs, for (Ga,In)P lattice matched to straight GaAs, as determined in the present work.

per end of this range. (ii) For $0.27 < x < 0.47$, the system should be a staggered one, with (Ga,In)P having both bands below those of $Al_xGa_{1-x}As$. The residual interface gap should increase slowly through this range, from about 1.78 eV for $x = 0.27$ to 1.95 eV for $x = 0.47$. This might be an interesting range for the study of staggered-lineup luminescence[19,20] in p-$Al_xGa_{1-x}As$/n-(Ga,In)P heterojunctions. (iii) For $x > 0.47$, the band lineup would become straggling again, but now with (Ga,In)P having the smaller energy gap.

It would appear that these band lineups might find applications in future electronic and optoelectronic device structures. With regard to the initial motivation for this work, the use of (Ga,In)P/GaAs HJs as emitters in HBTs, both our data and the recent reassessments of the band lineups within the $Al_xGa_{1-x}As$ alloy system[18] diminish somewhat the attractiveness of that idea: The conduction-band offsets in the (Ga,In)P/GaAs system are not quite as small as had been hoped, and those within the $Al_xGa_{1-x}As$ alloy system are not as large as had been feared. Together with the more difficult technology of (Ga,In)P relative to (Al,Ga)As, these changes conspire to reduce the incentive for (Ga,In)P as a material for HBTs, but probably not for other applications.

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AD-A188 137 DEVELOPMENT OF A PLANAR HETEROJUNCTION BIPOLAR TRANSISTOR FOR VERY HIGH S..(U) CALIFORNIA UNIV SANTA BARBARA DEPT OF ELECTRICAL AND COMPUTER.. 2/2

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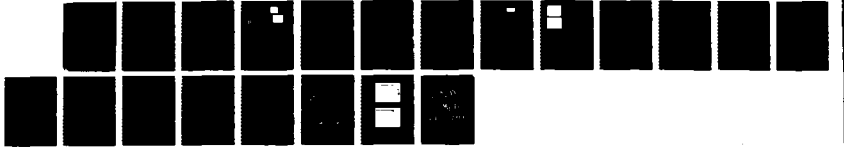

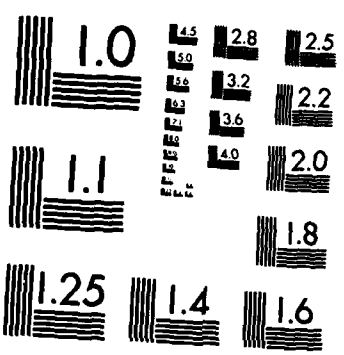

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Heterojunction Bipolar Transistor Using a (Ga,In)P Emitter on a GaAs Base, Grown by Molecular Beam Epitaxy

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Abstract—We report the first N-p-n heterojunction bipolar transistor (HBT) using a (Ga,In)P/GaAs heterojunction emitter on a GaAs base. This combination is of interest as a potential alternate to (Al,Ga)As/GaAs, because of theoretical predictions of a larger valence band discontinuity and a smaller conduction band discontinuity, thus eliminating the need for grading of the emitter/base junction. The structure was grown by molecular beam epitaxy, with the base doping ($\sim 10^{19}$cm^{-3}) far exceeding the n-type doping ($\sim 5 \cdot ^{17}$cm^{-3}) of the (Ga,In)P wide gap emitter (E_g = 1.88 eV). Common-emitter current gains of 30 were attained at a current density of 3000 A/cm^2, the highest current density achieved without burnout.

I. INTRODUCTION

HETEROJUNCTION BIPOLAR TRANSISTORS (HBT's) have stimulated much interest due to their predicted potential for high current gain and superior high-frequency performance [1], [2]. By utilizing an emitter with a wider energy gap than that of the base, the majority carriers of the base can be more strongly confined to this region. This confinement can be utilized to achieve high emitter efficiencies even in the presence of a (desirable) very high base-to-emitter doping ratio. To achieve this end it is, however important to minimize any electron blocking "spike barrier" in the conduction band, as it may occur at an abrupt emitter/base heterojunction if the band lineup at the latter is such that a large fraction of the total energy gap discontiuity occurs in the conduction band rather than in the valence band. It has been pointed out [1] that the overall effect of a fully developed spike is roughly the same as if the energy gap in the emitter were increased only by the amount of the valence band discontinuity ΔE_v rather than by the full energy gap discontinuity. An additional drawback of the conduction band spike is an undesirable increase in the emitter turnon voltage by about $\Delta E_v/q$.

The Ga-As based HBT work up to now has concentrated solely on GaAs paired with (Al,Ga)As. This dominance is due to that material system's inherent lattice matching, which yields interfaces of low defect densities. The energy band lineup in the (Al,Ga)As/GaAs system is, however, less than ideal because of the unfavorable band lineup: about 62 percent of the energy gap difference occurs in the conduction band [4], causing an undesirable potential barrier to electron injection from the emitter. A!though compositional grading of the emitter–base junction can alleviate this drawback [5], a heterojunction with a majority of its energy gap discontinuity in the valence band would be much more desirable.

The (Ga,In)P/GaAs system has been proposed as such an alternate for GaAs-based HBT's [6]. A linear interpolation between the theoretical band offsets predicted by the Harrison theory [7] of band lineups for GaP/GaAs and InP/GaAs heterojunctions yields a valence-band offset of 0.29 eV and a conduction-band offset of 0.16 eV for the lattice-matched $Ga_{0.51}In_{0.49}P$/GaAs heterojunction. It is not clear exactly how reliable these specific numerical values are, but the Harrison theory tends to describe at least the general trends of band lineups very well, and we therefore believe that the overall prediction of a substantially larger valence-band offset than conduction-band offset is probably reliable. In this letter, we present what we believe to be the first report on the fabrication of a (Ga,In)P/GaAs HBT, and the demonstration of the wide-gap emitter effect in this material system.

II. MBE GROWTH AND DEVICE FABRICATION

The epitaxial layers of the HBT reported here were grown by MBE in a Varian MBE 360 system. A (100)-oriented GaAs substrate, Si-doped to 10^{18} cm^{-3}, was used. At a substrate temperature of 560°C, a 0.25-μm-thick GaAs collector, non-intentionally doped n-type to 10^{16} cm^{-3}, was grown directly on the substrate, followed by a 0.15-μm-thick GaAs base, p-type doped with Be to 10^{19} cm^{-3}. This was followed by the growth of the (Ga,In)P emitter.

The MBE technology of the (Ga,In)P/GaAs system is relatively undeveloped [8][1], [9], with lasers being the only kind of device reported so far [10] In our procedure, separate Ga and In sources and a novel P_2 source were utilized to grow the (Ga,In)P emitter layer. The P_2 source consisted of a GaP decomposition source [11], modified with a baffle to condense out the undesired Ga flux component [12]. Once proper Ga and In fluxes were obtained, as determined by ion gauge measurements at the substrate

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[1] This paper [8] contains references to most of the earlier work in this system.

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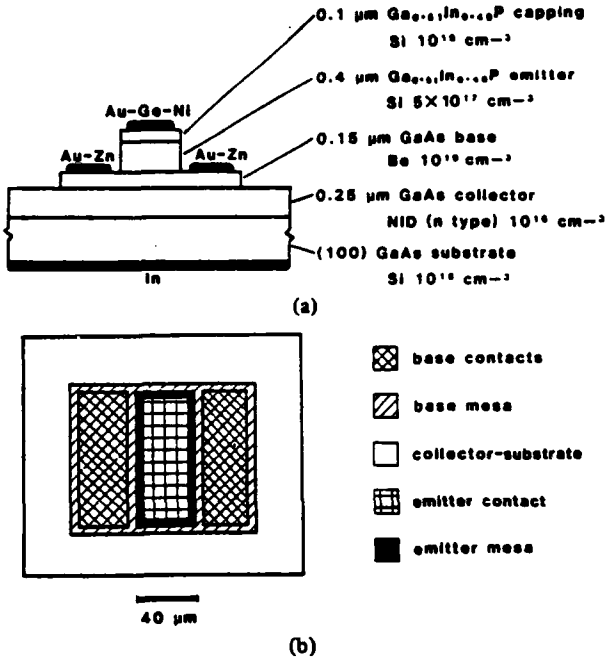

Fig. 1. Heterojunction bipolar transistor. (a) Schematic cross section. (b) Scaled top view.

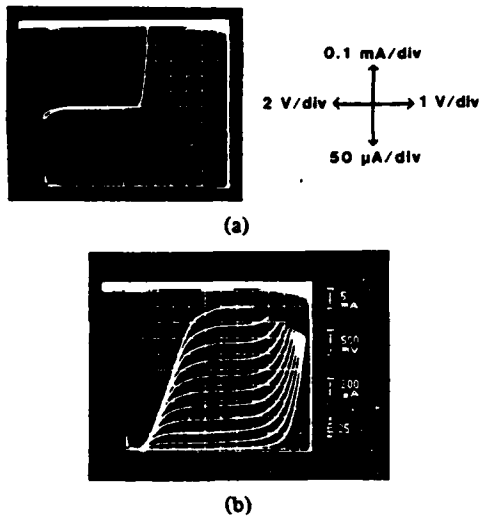

Fig. 2. (a) I-V characteristics of GaAs/(Ga,In)P p-N base/emitter heterojunction. (b) Common-emitter characteristics of (Ga,In)P/GaAs heterojunction bipolar transistor.

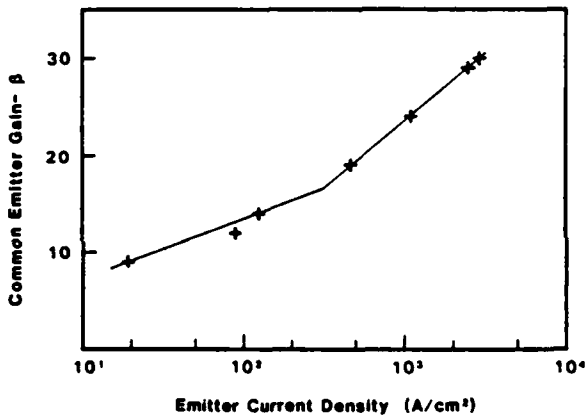

Fig. 3. Common-emitter current gain versus emitter current density. The two straight lines drawn through the data and the kink represent an ad hoc fit; they have no theoretical basis.

position, the substrate temperature was reset to 510°C. Using a P_2 beam of 3×10^{-6} torr, a 0.4-μm-thick $Ga_{0.51}In_{0.49}P$ layer, n-type doped with Si to 5×10^{17} cm^{-3}, was grown at a rate of 0.5 μm/h. The Si doping was then increased to 10^{18} cm^{-3} for another 0.1 μm, for ohmic contact to the emitter. Note that the base doping exceeded that of the emitter by over an order of magnitude.

Discrete transistors with relatively large lateral dimensions were fabricated from the grown wafer using the mesa structure in Fig. 1(a) and (b). The reason for the large dimensions was to keep the processing of the nonstandard wafers as simple as possible. The emitter was contacted with evaporated Au-Ge-Ni. The emitter mesa was then defined by selectively etching down to the GaAs base with HCl. Au–Zn base contacts were evaporated to the exposed p-type GaAs, and the base mesa was etched using H_2SO_4:H_2O_2:H_2O = 10:3:87. The contacts were then alloyed at 450°C for 1 min. in a H_2:N_2 = 15:85 gas mixture. The collector was contacted with In on the backside of the substrate, which thus served as a portion of the device. The emitter–base and collector–base junction areas were 3.2×10^{-5} cm^2 and 9.6×10^{-3} cm^2.

III. RESULTS AND DISCUSSION

A typical I-V characteristic of the p-GaAs/N-(Ga,In)P base/emitter heterojunction is shown in Fig. 2(a). The diodes have ~1.0-V forward current turn-on voltages, with hard breakdown between 12- and 14-V reverse bias. The low current turn-on voltage supports our speculation that there is a much lower conduction-band spike barrier in this system than in ungraded (Al,Ga)As/GaAs emitter/base junctions.

In Fig. 2(b), the common-emitter characteristics of a typical HBT are shown, and Fig. 3 gives the current gain β as a function of emitter current density. It can be seen that the current gains are low at low current densities, but increase strongly with increasing density. This behavior suggests that appreciable space-charge layer recombination takes place at the emitter/base junction, presumably due to defects at the still-imperfect heterojunction interface. At high current densities this defect current is swamped by the injection current, which increases more strongly with forward bias—like exp (qV/kT)—than the defect current. Due to burnout problems, we were unable to achieve current densities above a relatively low 3000 A/cm^2 in these first and still excessively large devices. At these densities, β-values of 30 were obtained, still increasing with current, and suggesting that much higher β-values could be achieved if the current densities could be raised, even for the present defect current densities.

The current densities were limited by what appeared to be "forward secondary breakdown" [14], leading to a burning out of the device. Device failure was characterized by the collector shorting to the emitter. The shorted emitter/collector combination showed degraded but still rectifying I-V characteristics against the base. The formation

of the short circuit was often preceded by gain instability, symptomatic of thermal effects. Power calculations assuming uniform dissipation suggest a junction temperature less than 65°C at room temperature ambient. Hence, the heating is attributed to localized thermal runaway, perhaps caused by localized defects at the (Ga,In)P/GaAs interface.

The relatively large geometries of the devices prevented the determination of the high-frequency characteristics. The dc performance was also degraded by the large dimensions of the device, which caused emitter current crowding effects.

The current gain of this nonoptimized HBT is at present far below the gains achieved with the more highly developed (Al,Ga)As/GaAs material system [3], [5], [13], but is comparable to the first (Al,Ga)As/GaAs HBT reported [15]. As indicated, the current gain characteristics of Fig. 3 imply that higher gains than 30 should be achievable, but the failure mechanism indicates that materials problems still exist. Further improvement of the growth parameters, particularly an increase of the substrate temperature, is expected to increase the injection efficiency and current handling capabilities of the (Ga,In)P/GaAs heterojunctions.

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An (Al,Ga)As/GaAs Heterostructure Bipolar Transistor with Nonalloyed Graded-Gap Ohmic Contacts to the Base and Emitter

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An (Al,Ga)As/GaAs Heterostructure Bipolar Transistor with Nonalloyed Graded-Gap Ohmic Contacts to the Base and Emitter

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Abstract—**Graded regions of n-(Ga,In)As and p-Ga(As,Sb) were incorporated side-by-side as emitter and base contacts, respectively, into an n-p-n (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT). The process involved two separate molecular beam epitaxy (MBE) growths, leading to base contact regions that were self-aligned to the emitter mesas. The devices could be easily probed with pressure contacts even prior to any metallization, and excellent characteristics were obtained after final metallization. Contact resistivities of 5×10^{-7} and 3×10^{-6} $\Omega \cdot cm^2$ were measured for n- and p-type graded-gap ohmic contact structures, respectively.**

I. Introduction

In 1981, Woodall *et al.* [1] proposed and demonstrated a nonalloyed graded-gap scheme for obtaining ohmic contacts to n-type GaAs, by first growing a graded transition from GaAs to InAs and then making a nonalloyed metallic contact to the InAs. The underlying idea was as follows. It is well known that at a metal-to-InAs interface the Fermi level is pinned inside the InAs conduction band [2], hence this interface by itself acts as an ideal negative-barrier ohmic contact. However, if the GaAs-to-InAs transition were not graded, it would act as a quasi-Schottky barrier with a barrier height close to the conduction-band offset ΔE_c of the GaAs/InAs heterojunction, about 0.9 eV [3], and the contact would be poor overall. Sufficient grading flattens out the heterojunction barrier, and leads to an excellent ohmic contact with properties that make it an attractive alternative to the widely used Au/Ge/Ni/Au alloyed system [4]–[6]. For p-type GaAs, the Ga(As,Sb) system could be similarly used, as proposed by Chang and Freeouf [7].

In the present work, we report the side-by-side incorporation of such n- and p-type graded-gap contacts as emitter and base contacts of an n-p-n (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT). Not only are the contact resistivities competitive with those of alloyed contacts, but the nonalloyed contacts are noninvasive. They are, therefore, particularly attractive for bipolar transistors, because emitter regions can be employed that are much thinner than those possible with alloyed contacts, leading to reduced emitter resistances. Also, the possibility of alloying through the thin base region is eliminated with nonalloyed base contacts.

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II. Graded-Gap Contact Growth Procedure

As a preliminary to transistors, n- and p-type graded-gap contacts grown by molecular beam epitaxy (MBE) on (100)-oriented semi-insulating GaAs substrates were investigated separately. To keep the series path resistance of the graded region low, the doping in the graded region should be as high as possible and the graded region should be as narrow as possible, limited only by the requirement to flatten the quasi-Schottky barrier mentioned in the introduction. Theoretical investigations [8] show that graded regions as narrow as 30 nm should be permissible. For the n-type graded-gap contact structures, approximately 200 nm of 1×10^{18} cm^{-3}(Si-doped) n^+-GaAs was grown at 600°C, followed by approximately 30 nm of n^+-(Ga,In)As compositionally graded from GaAs to InAs. The grading was achieved by ramping the temperatures of the Ga and In furnaces. In addition, during the growth of the graded region the substrate temperature was ramped down from 600°C to 500°C because the temperature of congruent sublimation for (Ga,In)As decreases with increasing indium fraction [9]. Approximately 30 nm of n^+-InAs was grown above the graded region. The doping level in the graded region and the InAs was about 3×10^{18} cm^{-3}.

For the p-type graded-gap contact structures, a 200-nm p^+-GaAs buffer layer was grown first, followed by 30-nm p^+-Ga(As,Sb) compositionally graded from GaAs to GaSb. The growth of the graded region was initiated by opening the shutter of the Sb source. Both the antimony-to-gallium and the *initial* arsenic-to-gallium *atomic* flux ratios were approximately 3:1. In the presence of such an arsenic flux at a substrate temperature of 600°C, very little (< 1 percent) antimony gets incorporated into the growing material [10]. During the growth of the graded region the substrate temperature was then ramped from 600°C to 470°C, for two reasons.

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1) The temperature of congruent sublimation of GaSb is approximately 455°C [9] which is much lower than that of GaAs. Consequently GaSb requires a lower growth temperature than GaAs. 2) The substitution of arsenic by antimony is enhanced at lower growth temperatures [10], thus facilitating the growth of the graded layer. In addition, to accomplish a complete transition to GaSb, the power to the arsenic furnace was turned off 3 min into the growth of the graded region. The arsenic flux dropped to a tenth of its initial value at the end of the growth of the graded region, while the antimony flux remained constant. About 30 nm of p^+-GaSb was grown above the graded layer. The p^+-layers were doped with Be to about 5×10^{18} cm^{-3}.

III. Contact Resistivity Measurements

The specific contact resistivities of the n- and p-type graded-gap contacts were measured with a four-point Kelvin cross-resistor structure [11]. For nonalloyed (Ga,In)As graded-gap contacts to n-GaAs, contact resistivities down to 5×10^{-7} $\Omega \cdot$cm^2 were obtained. For p-type Ga(As,Sb) graded-gap contacts, resistivities down to 3×10^{-6} $\Omega \cdot$cm^2 were measured. However, the Kelvin measurement technique is extremely sensitive to misalignment between the mesa and the ohmic metal [12]. In general, the measurement overestimates the contact resistivity and it is this pessimistic upper limit that is reported here. The true value of the resistivity could be much lower than the measured value.

For comparison, the typical values for Au/Ge/Ni n-type and Au/Zn p-type alloyed contacts found in the literature are 1×10^{-6} $\Omega \cdot$cm^2 [5] and 7×10^{-6} $\Omega \cdot$cm^2 [13]. It can be seen that our measured values are competitive with the typical values reported in the literature.

IV. Transistors

The HBT structure was grown by MBE on a (100)-oriented n^+-GaAs substrate. The doping levels, compositions, and thicknesses of the initial HBT layers are shown in Fig. 1. The region between the base and the emitter was digitally graded with a narrow-well (Al,Ga)As/GaAs superlattice [14]. The Al mole fraction in the (Al,Ga)As emitter was 0.25. The GaAs was grown at 600°C, and the (Al,Ga)As at 650°C, with arsenic-to-group III *atomic* flux ratios of approximately 2:1. The growth temperature was reduced to 600°C at the end of the emitter layer, and 30 nm of (Al,Ga,In)As compositionally graded from (Al,Ga)As to InAs was grown, followed by 30 nm of InAs, using a procedure similar to the one described for the growth of the (Ga,In)As graded-gap contact in Section II. The graded region and the InAs were heavily doped n-type with Si to about 3×10^{18} cm^{-3}.

The sample was then removed from the MBE system and SiO_2 was deposited using plasma-enhanced chemical vapor deposition (PCVD) at 300°C. The SiO_2 was patterned into the emitter mesa regions using standard photoresist techniques. The SiO_2 was used as a mask for etching the emitter mesas, with H_3PO_4:H_2O_2:H_2O = 4:1:50. The sample was then rinsed in solvents, rinsed in deionized water for 10 min, and reloaded into the MBE system for the base contact regrowth.

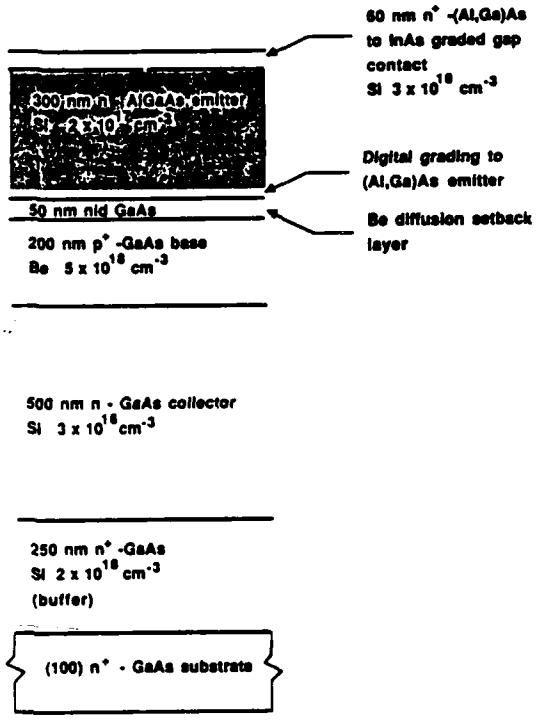

Fig. 1. Heterostructure bipolar transistor layer diagram. The structure was grown by MBE.

The oxide was desorbed at approximately 620°C in an arsenic ambient. A small carbon peak was detected by Auger electron spectroscopy after the oxide desorption. Approximately 100 nm of p^+-GaAs was grown to smooth out the restart interface. Then 30 nm of p^+-Ga(As,Sb) compositionally graded from GaAs to GaSb was grown, followed by 30 nm of p^+-GaSb, as described in Section II. The doping in the p^+-layers was about 5×10^{18} cm^{-3}. Because of the undercut due to the emitter mesa etch, the MBE regrowth of the p-type contacts leads to base contact regions that are self-aligned with respect to the emitter mesas, a very desirable feature.

One of the potential advantages of graded-gap contacts is that they are capable of withstanding high-temperature processing. Our growth procedure showed that the (Ga,In)As capped with SiO_2 could clearly withstand high temperatures of 620°C during the regrowth of the p-type graded-gap contact.

After the sample was removed from the MBE system the material grown on top of the SiO_2 was found to be polycrystalline. Furthermore, it appeared to be penetrated by an HF etch: the SiO_2 was easily etched off with HF, along with the material on top of the SiO_2. Base mesas were then etched, first using $HF:H_2O_2:H_2O$ = 10:1:100 to etch the Ga(As,Sb) and then using the phosphoric acid-based etch mentioned above to etch the GaAs. At this point the device I–V characteristics could be obtained even prior to any final metallization, using tungsten probe tips to directly contact the semiconductor surfaces of the base and the emitter. Indium alloyed on the backside of the n^+-wafer formed the collector contact. Examples of I–V curves obtained in this manner are shown in Fig. 2(a).

Finally, a dielectric (SiO_2) was deposited by PCVD, contact

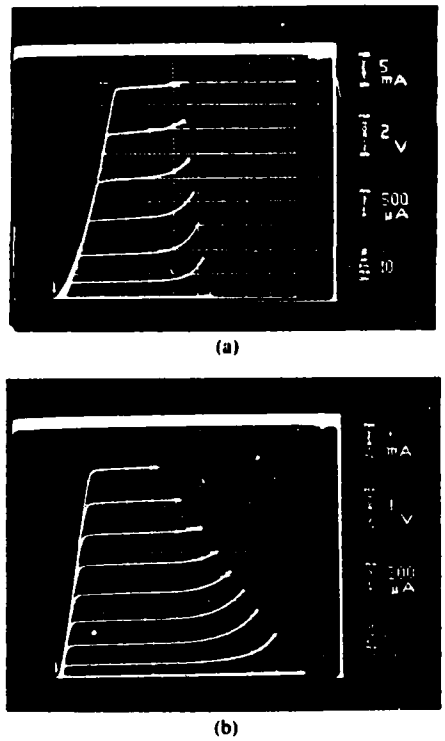

Fig. 2. Transistor I–V curves obtained (a) prior to metallization. Emitter area is 150 × 150 μm^2. (b) After final metallization. Emitter area is 20 × 20 μm^2. These transistors were from a different run than those corresponding to (a).

windows were cut, and Cr/Au metallization was deposited by evaporation. Both the base and the emitter metallization were done in one step. No alloying was done. The device I–V curves obtained after final metallization are shown in Fig. 2(b). It should be noted that the I–V curves in Fig. 2(b) were obtained on devices fabricated in a different run than those corresponding to Fig. 2(a). The I–V curves were very similar to those obtained on conventional alloyed contact transistors which were fabricated in a different run.

Acknowledgment

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AlGaAs/GaAs heterostructure bipolar transistor with non-alloyed graded-gap ohmic contacts to the base and emitter

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One of the most troublesome areas of compound semiconductor technology is that of the ohmic contacts. In 1981, Woodall et al. [1] proposed and demonstrated a non-alloyed graded-gap scheme for obtaining ohmic contacts to n-type GaAs, by first growing a graded transition from GaAs to InAs and then making a non-alloyed metallic contact to the InAs. A theoretical analysis shows that specific contact resistivities as low as $2 \times 10^{-9}\Omega cm^2$ should be possible for n-type ohmic contacts with doping levels of $10^{19}cm^{-3}$ in the (Ga,In)As. Analogously, the Ga(As,Sb) system can be used for p-type ohmic contacts, for which resistivities down to $2 \times 10^{-8}\Omega cm^2$ should be achievable.

We have grown such graded gap structures by MBE and have obtained resistivities down to $5 \times 10^{-8}\Omega cm^2$ for n-type contacts and $3 \times 10^{-6}\Omega cm^2$ for p-type contacts. These values are higher than those predicted possible by our analysis, because the graded layers were not fully optimized, and doping levels of $10^{19}cm^{-3}$ were not obtained. However, the values are considerably better than typically observed with the widely used Au/Ge/Ni and Au/Zn alloyed contacts. Both kinds of graded-gap contacts were incorporated side-by-side into n-p-n AlGaAs/GaAs heterostructure bipolar transistors (HBTs). The advantages of graded-gap contacts in a HBT are: (a) a greatly reduced base and emitter contact resistance, (b) non-invasiveness, and (c) the base and emitter metallizations can be performed in one step. A n^+-graded gap (Ga,In)As contact layer was grown above the heterojunction emitter. The sample was then removed from the MBE system and SiO_2 was deposited, patterned into the emitter regions, and emitter mesas were etched. After reloading, approximately 100nm of p^+-GaAs were grown, followed by 35nm of graded Ga(As,Sb). The regrown layer on top of the SiO_2 was removed by dissolving the SiO_2. The devices could be probed using tungsten probe tips *directly* contacting the semiconductor surfaces of the base and emitter with the n^+-substrate forming the collector contact. The devices showed excellent transistor action, with current gains of 20, and no sign of significant contact resistance even prior to any metallization.

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A Self-Aligned AlGaAs/GaAs Heterostructure Bipolar Transistor with Non-Alloyed Graded-Gap Ohmic Contacts to the Base and Emitter

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I. Introduction

A nonalloyed graded-gap scheme for obtaining ohmic contacts to n-type GaAs, by first growing a graded transition from GaAs to InAs and then making a nonalloyed metallic contact to the InAs, was proposed by Woodall et al. [1]. The underlying idea was as follows. A metal-to-InAs interface acts as an ideal negative-barrier ohmic contact because the Fermi level is pinned inside the InAs conduction band, as shown in Fig. 1. However, if the GaAs-to-InAs transition were not graded, it would act as a quasi-Schottky barrier, and the contact would be poor overall. Sufficient grading flattens out the heterojunction barrier and leads to an excellent ohmic contact with properties that make it an attractive alternative to the widely used Au/Ge/Ni/Au alloyed system. For p-type GaAs, the Ga(As,Sb) system could be similarly used, as proposed by Chang and Freeouf [2].

Graded-gap ohmic contacts are now beginning to be incorporated in heterostructure bipolar transistors (HBTs). In 1986, we demonstrated the first (Al,Ga)As/GaAs HBT that had non-alloyed graded-gap contacts to *both* the emitter and the base [3], [4]. A n^+-graded (Ga,In)As layer was used as the emitter contact, and p^+-Ga(As,Sb) formed the base contact. Self-aligned HBTs employing graded-gap contacts to only the emitter, with the emitter cap layer graded to $Ga_{0.5}In_{0.5}As$, have also been reported [5], [6]. Most recently, using such self-aligned HBTs, Nagata *et al.* [7] demonstrated ring oscillators that had a propagation delay of 5.5ps/gate, with the HBTs themselves having f_T's of 80 GHz and f_{max}'s of 60 GHz.

The contact resistivities of graded-gap contacts are competitive with

those of alloyed contacts, and the nonalloyed contacts are non-invasive. They are, therefore, particularly attractive for HBTs, because emitter regions can be employed that are much thinner than those possible with alloyed contacts, leading to reduced emitter resistances. Also, the possibility of alloying through the thin base region is eliminated with nonalloyed base contacts. A further advantage of side-by-side incorporation of both n- and p-type graded-gap contacts into a HBT is that the base and emitter metallizations can be performed in one step, which makes it possible to fabricate self-aligned HBTs. In the present work, we demonstrate such a self-aligned HBT.

II. MBE Growth of Graded-Gap Contacts and Contact Resistivity Measurements

Both n- and p-type graded-gap contacts were grown by molecular beam epitaxy (MBE) on (100)-oriented semi-insulating GaAs substrates for contact resistivity measurements. Our earlier work [4] contains a description of the growth procedure, the salient features of which are as follows.

For the n-type graded-gap contact structures, approximately 200 nm of $1 \times 10^{18} cm^{-3}$ (Si-doped) n^+ -GaAs was grown at 600°C, followed by approximately 30 nm of n^+ -(Ga,In)As compositionally graded from GaAs to InAs. During the growth of the graded region, the substrate temperature was ramped down from 600°C to 500°C. Approximately 30 nm of n^+ -InAs was grown above the graded region. The doping level in the graded region and the InAs was about $3 \times 10^{18} cm^{-3}$.

For the p-type graded-gap contact structures, a 200 nm p^+ -GaAs buffer layer was grown first, followed by 30 nm p^+ -Ga(As,Sb) compositionally graded from GaAs to GaSb. The substrate temperature was ramped from 600°C to 470°C during the growth of the graded region. About 30 nm of p^+ -GaSb was grown above the graded layer. The p^+ -layers were doped with Be to about $5 \times 10^{18} cm^{-3}$.

The specific contact resistivities of the n- and p-type graded-gap contacts were measured by the standard TLM method. For nonalloyed

(Ga,In)As graded-gap contacts to n-GaAs, contact resitivities down to $5 \times 10^{-7}\ \Omega\ cm^2$ were obtained. For p-type Ga(As,Sb) graded-gap contacts, resistivities down to $3 \times 10^{-6}\ \Omega\ cm^2$ were measured. While our resistivity values are competitive with those of typical n- and p-type alloyed contacts, it must be noted that they can be reduced even further by achieving higher doping levels in the graded layers. For instance, Nittono *et al.* [8] have obtained contact resistivities as low as $5 \times 10^{-8}\ \Omega\ cm^2$ for layers graded to $Ga_{0.35}In_{0.65}As$ and doped to $1.5 \times 10^{19}\ cm^{-3}$.

III. Transistors

The HBT structure was grown by MBE on a (100)-oriented, semi-insulating GaAs substrate. The doping levels, compositions, and thicknesses of the initial HBT layers are shown in Fig. 2. The region between the base and emitter was graded from GaAs to (Al,Ga)As over 30nm. The Al mole fraction in the emitter was 0.3. The GaAs was grown at 600°C, and the (Al,Ga)As at 650°C with arsenic-to-group III *atomic* flux ratios of approximately 2:1. At the end of the emitter layer, 30 nm of n^+-(Al,Ga)As graded to GaAs was grown, and the growth temperature was reduced to 600°C. Then, the n^+-(Ga,In)As graded-gap contact layer was grown, as described in section II above.

The process sequence for the self-aligned HBTs is shown in Fig. 3, and was as follows. The sample was removed from the MBE system and SiO_2 was deposited using plasma-enhanced chemical vapor deposition (PCVD) at 300°C. The SiO_2 was patterned into the emitter mesa regions using standard photoresist techniques, and the emitter stripes were oriented so that they were parallel to the ⟨110⟩ direction of the crystal. The SiO_2 was used as a mask for etching the emitter mesas. The (Ga,In)As contact layer was etched with HCl, and the emitter mesa with $NH_4OH : H_2O_2 : H_2O$ (3 : 1 : 50). The NH_4OH based etch produced inward sloping sidewalls ("reverse-mesas") as reported by Fischer *et al* [9]. The sample was rinsed in deionized water for 10 min, and reloaded into the MBE system for base contact regrowth.

After desorption of the oxide at approximately 620°C in an arsenic ambient, 50nm of p^+ - GaAs was grown to smooth cut the restart interface.

The Ga(As,Sb) graded-gap contact was then grown as described in Section II. During regrowth the SiO_2 acts as a cap for the n-(Ga,In)As contact and prevents its degradation. The overhang of the SiO_2 on the emitter mesa prevents growth on the sidewalls, and leads to Ga(As,Sb) regions that are self -aligned with the emitter mesas.

The regrown layer on top of the SiO_2 was removed by dissolving the SiO_2 in HF. Next, 40nm of Ni was deposited on the base and emitter surfaces. During metal deposition, the shadow created by the reverse-mesa prevents the base and emitter contacts from being shorted and leads to base contacts that are self-aligned with the emitter contacts. The separation between the regrown Ga(As,Sb) and the emitter mesa edge is determined by the undercut beneath the SiO_2 and is about 250nm. The separation between the base and emitter contact metal is much less than 250nm because this distance is determined by the shadow produced by the reverse mesa. After the base and collector mesas were etched, the collector contact was formed with alloyed Au-Ge/Ni/Au. Photosensitive polyimide was used as a dielectric, and final metallization was done with Ti/Au.

The device I/V curves obtained after final metallization are shown in Fig. 4. The emitter stripe dimension was 7μm x 25μm, and the HBT had a current gain of 15 at collector current densities of about 15 kA/cm^2.

IV. Calculated high frequency performance

For a base width of 0.15μm, base doping of 5×10^{18}cm^{-3} and an assumed hole mobility of 100cm^2/Vsec, the base sheet resistance is calculated to be 830 Ω/□. As mentioned in section III above, the self-aligned HBTs have a base-to-emitter contact separation of 0.25μm. The majority carriers must travel this distance, and an additional average distance 1/4 • W = 1.75μm under the emitter, W being the emitter width (7μm in the present case). The sides of the emitter total 50μm, and the base resistance is estimated to be 30Ω. For our device geometry, the base-collector area is approximately 20μm x 25μm, and the base-to-collector capacitance is calculated to be 0.17pF. Assuming an electron mobility of 1000cm^2/Vsec in the base, the base transit time is calculated to

be 4.3ps. Using these values and the standard equations for the gain-bandwidth frequency (f_T), and the maximum frequency of oscillation (f_{max}) [10], the calculated f_T and f_{max} values for this device are : f_T = 37GHz and f_{max} = 17GHz. Improved device performance can be expected for emitter stripe widths narrower than 7μm, and for reduced base-to-collector areas.

V. Acknowledgements

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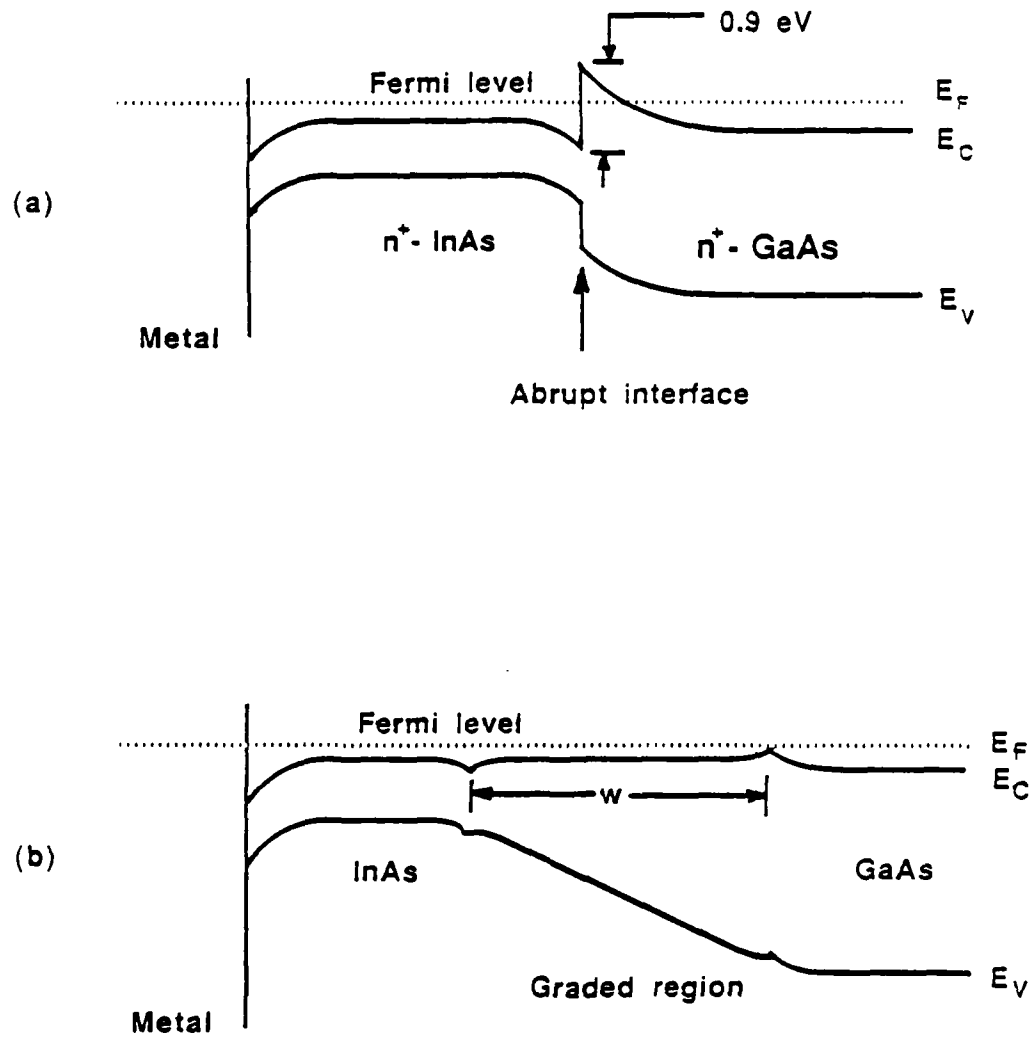


Fig. 1 Band diagrams for (a) an abrupt GaAs/InAs interface, and (b) a graded GaAs/InAs interface

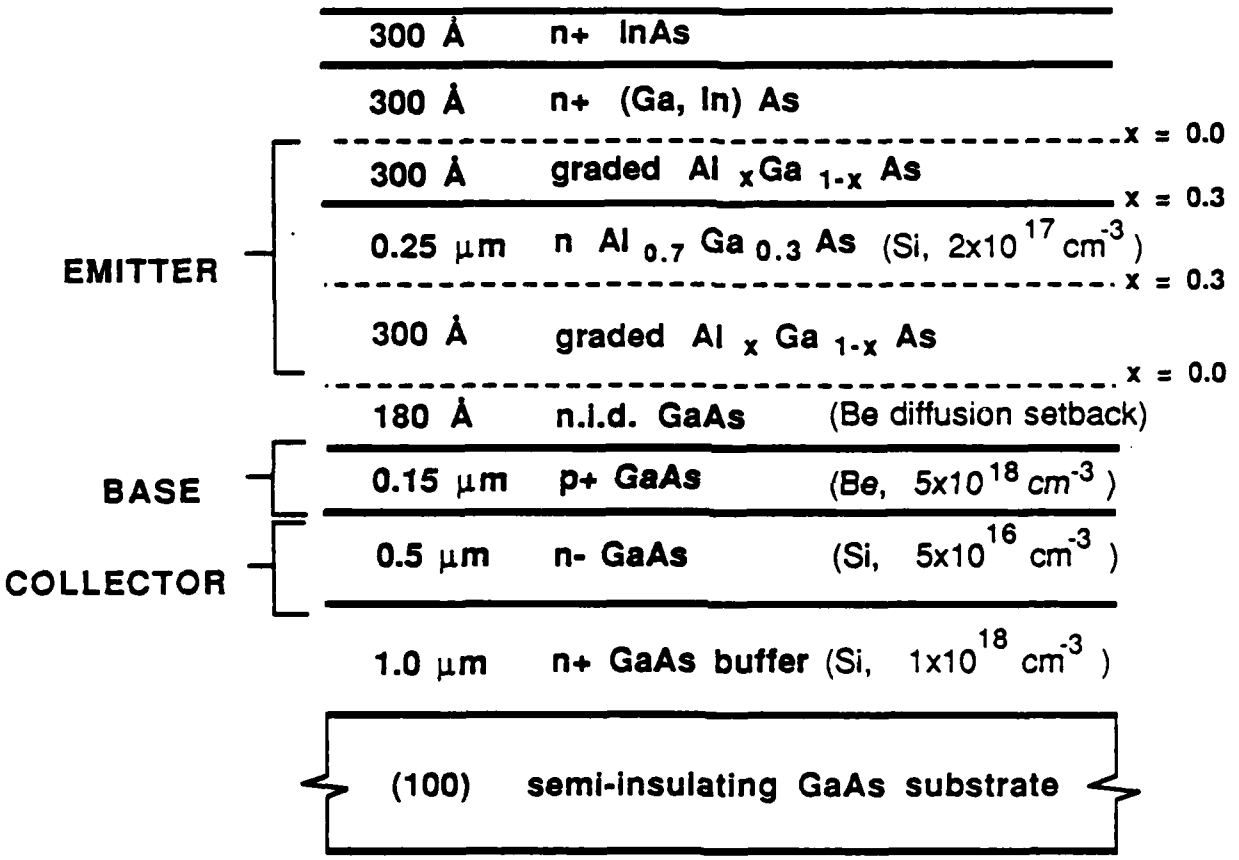


Fig. 2 AlGaAs/GaAs HBT layer diagram..

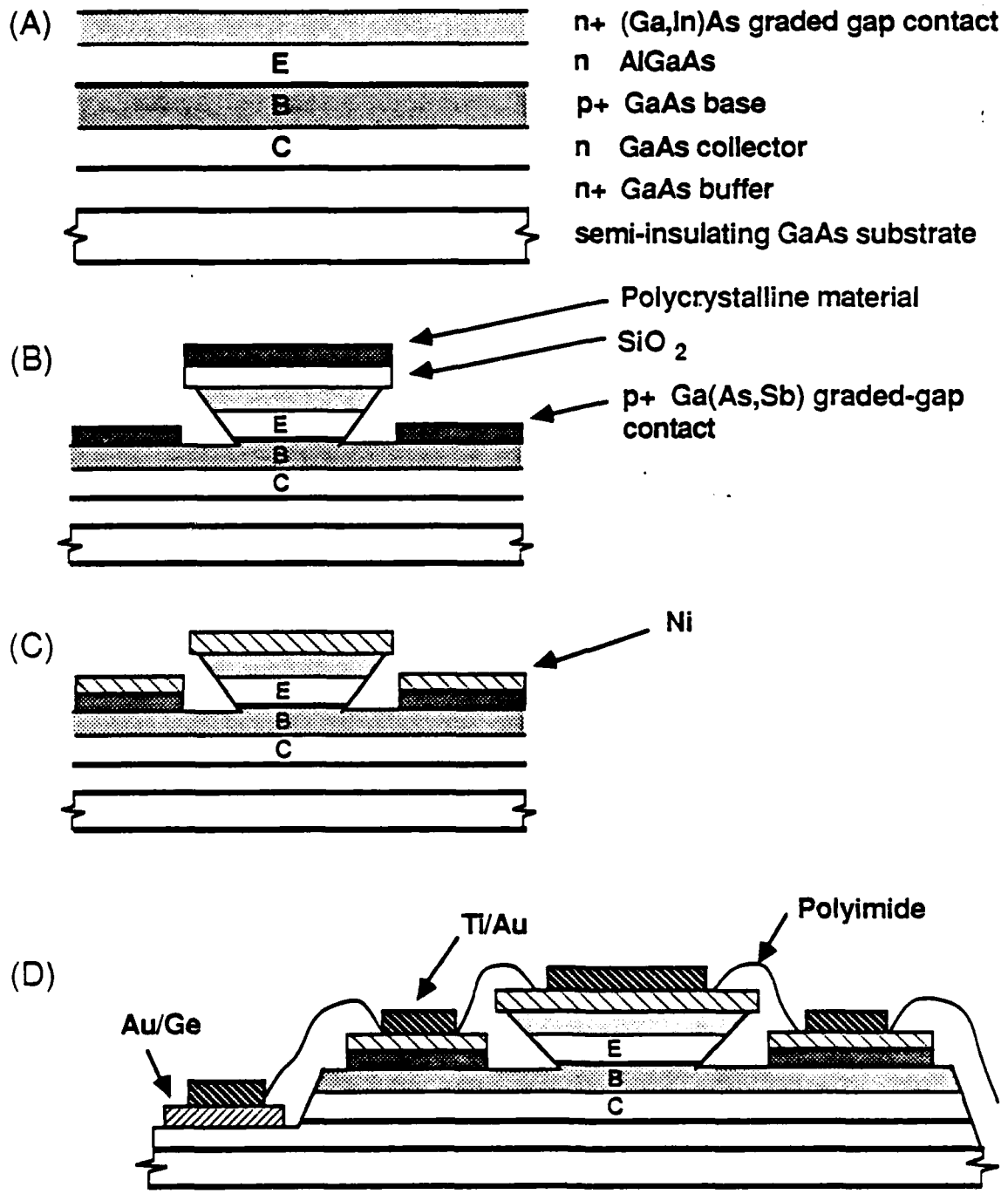
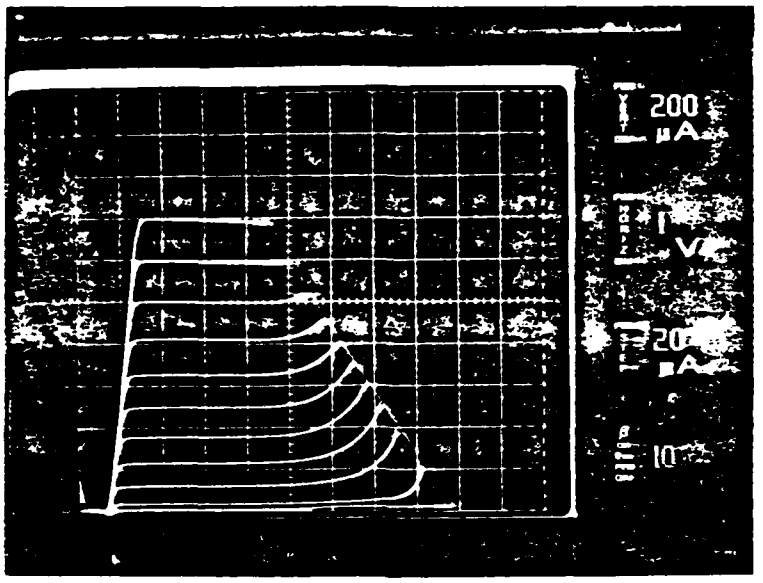


Fig. 3 Self-aligned HBT process sequence. (A) MBE grown structure, (B) Emitter mesa etch followed by base regrowth, (C) Self-aligned metal deposition, and (D) completed structure.

(a)



(b)

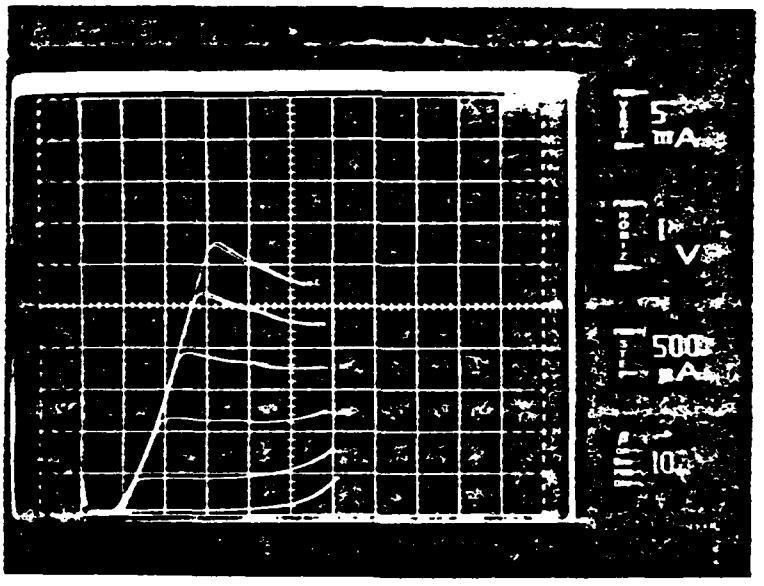


Fig. 4 I-V characteristics of the self-aligned HBT (emitter area = 7μm x 25μm) for (a) low and (b) high collector current densities

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